IEEE SOLID-STATE CIRCUITS SOCIETY

ADVANCE PROGRAM



2026 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 15, 16, 17, 18, 19

CONFERENCE THEME:

ADVANCING AI WITH IC & SOC INNOVATIONS

SAN FRANCISCO MARRIOTT MARQUIS HOTEL

DRAFT 2-12-2026

5-DAY PROGRAM

SUNDAY ALL-DAY

2 FORUMS: POWER EFFICIENT CIRCUITS & SYSTEMS FOR NEXT-GEN AGENTIC AI & ROBOTICS; ELECTRICAL & OPTICAL LINKS TOWARDS 400G+ CONNECTIVITY

10 TUTORIALS: FUNDAMENTALS OF ENERGY-EFFICIENT LDO REGULATOR; DESIGN TECHNIQUES FOR ROBUST & ENERGY-EFFICIENT BIOMEDICAL SYSTEM; FUNDAMENTALS OF COMPUTE-IN-MEMORY; PRINCIPLES & PRACTICES OF HIGH-SPEED D/A CONVERTER; MEMORY & DIGITAL CIRCUIT DESIGN BEYOND FINFET; INTERFERENCE MITIGATION TECHNIQUES IN WIRELESS; CLOCKING & CDR TECHNIQUES FOR HIGH-PERFORMANCE WIRELINE; DOHERTY POWER AMPLIFIER

2 EVENING EVENTS: BINGO NETWORKING; STUDENT RESEARCH PREVIEW

THURSDAY ALL-DAY

4 FORUMS: POWERING THE FUTURE OF AI/HPC/CHIPLET; THE RACE FOR 6G FR3 (7-24GHZ); ANALOG FOR AI & AI FOR ANALOG; CALIBRATION & DYNAMIC MATCHING TECHNIQUES FOR DATA CONVERTERS

SHORT-COURSE: CIRCUITS FOR OPTICAL SUBSYSTEMS: COMMUNICATIONS & BEYOND

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS

On Sunday, February 15th, the day before the official opening of the Conference, ISSCC 2026 offers:

- A choice of 10 Tutorials, or
- A choice of 1 of 2 all-day Advanced-Circuit-Design Forums:
  "Power Efficient Circuits & Systems for Next-Gen Agentic AI & Robotics"
  "Electrical & Optical Links Towards 400G+ Connectivity"

The 90-minute tutorials offer background information and a review of the basics in specific circuit- and system-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday, February 15th, there are three events: ***"Next Generation Circuit Designer 2026 Workshop"*** starting at 9:00 am and ***"Mentoring Session/Networking Bingo"*** will be offered starting at 4:00 pm. In addition, the Student-Research Preview (SRP), featuring sixty-second introductory presentations followed by a poster session from selected graduate-student researchers from around the world will begin at 8:00 pm. The SRP will start with an inspirational talk by Dr. Kinam Kim (Samsung).

On Monday, February 16th, ISSCC 2026 at 8:00 am offers four plenary papers on the theme: ***"Advancing AI with IC & SoC Innovations"***

On Monday at 1:30 pm, there are five parallel technical sessions, followed by a Social Hour at 5:30 pm open to all ISSCC attendees. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a Demonstration Session, featuring posters and live demonstrations of selected papers, along with a Corporate/Institution Exhibition

On Tuesday, February 17th, there are six parallel technical sessions, both morning and afternoon. Book Displays and Author Interviews will be accompanied by a second Demonstration Session. Tuesday evening includes two events, entitled:

"Generative AI for Silicon Design: Mastering Complexity, Democratizing Design, & Building Trust"

"The Augmented Human – Will Chips in Our Brain Enhance Our Cognitive Abilities?"

On Wednesday, February 18th, there will be five parallel technical sessions, both morning and afternoon, followed by Author Interviews.

On Thursday, February 19th, ISSCC offers a choice of five all-day events:

- A Short Course entitled:
  "Circuits for Optical Subsystems: Communications and Beyond"
- Four Advanced-Circuit-Design Forums entitled:
  "Powering the Future of AI, HPC, & Chiplet Architectures: From Dies to Package and Rack"
  "The Race for 6G FR3 (7-24GHz): From Network Deployment to System Integration & Breakthrough Technology"
  "Analog for AI & AI for Analog: What the Analog/RF People Can Do & Leverage in the AI Era"
  "Calibration and Dynamic Matching Techniques for High-Performance Data Converters"

This year, again, there is an option that allows an attendee to sample parts of all 5 Thursday offerings. Registration for educational events on Sunday and Thursday will be filled on a first-come first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for the Conference, Tutorials, Forums, and the Short Course.

Need Additional Information? Go to: www.isscc.org

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Optional Educational Events

ISSCC 2026 • Sunday, February 15th

Tutorials

8:30 AM

T1: Fundamentals of Energy-Efficient LDO Regulator Designs

T2: Fundamentals of Cryptography for Chip Designers: Classical to Post-Quantum

T3: Design Techniques for Robust and Energy-Efficient Biomedical Readouts

10:30 AM

T4: Fundamentals of Compute-in-Memory: From Circuits to Systems

T5: Fundamentals of Image Sensors: From Photon to Image

T6: Principles and Practices of High-Speed Digital-to-Analog Converter Design

1:30 PM

T7: Embedded Memory and Logic Circuit Design in Technologies Beyond FinFET

T8: Interference Mitigation Techniques in Wireless Communication Systems

3:30 PM

T9: Clocking and CDR Techniques for High-Performance Wireline Transceiver

T10: Doherty Power Amplifier: Fundamentals and Recent Advances

ISSCC 2026 • Sunday, February 15th

Forums

8:00 AM

F1: Power Efficient Circuits and Systems for Next-Gen Agentic AI and Robotics

F2: Electrical and Optical Links Towards 400G+ Connectivity

ISSCC 2026 • Sunday, February 15th

Morning Session - 9:00 AM

Next Generation Circuit Designer 2026 Workshop

Events Below are Included with your Conference Registration

ISSCC 2026 • Sunday, February 15th

Evening Events

4:00 PM to 6:00 PM:
Bingo Networking Event (Open to All)

8:00 PM

EE1: Student Research Preview: Short Presentations with Poster Session

ISSCC 2026 SCHEDULE OF EVENTS

Events Below are Included with your Conference Registration

ISSCC 2026 • Monday, February 16th Paper Sessions

8:30 AM	**Session 1:** Plenary - Invited Papers
1:30 PM	**Session 2:** Processors
1:30 PM	**Session 3:** Wearable and Wireless Biomedical Systems
3:35 PM	**Session 4:** Analog Techniques & Amplifiers
1:30 PM	**Session 5:** Sub-THz and mm-Wave Phased Arrays and Beamformers
3:35 PM	**Session 6:** Exploratory Receiver Architectures from GHz to THz
1:30 PM	**Session 7:** Image Sensors and Ranging
1:30 PM	**Session 8:** Die-to-Die and High-Speed Electrical Transceivers
3:35 PM	**Session 9:** Wireless Power

3:00 PM to 8:00 PM – Book Displays
3:00 PM to 8:00 PM – Corporations/Institution Exhibition
5:00 PM to 7:00 PM – Demonstration Session
5:30 PM – Author Interviews • Social Hour

ISSCC 2026 • Tuesday, February 17th Paper Sessions

8:00 AM	**Session 10:** Digital Processing and Circuit Techniques
8:00 AM	**Session 11:** Pipeline and Ultra-High-Speed Data Converters
8:00 AM	**Session 12:** Frequency Synthesizers and VCOs
8:00 AM	**Session 13:** Circuits for AI and AI for Circuits
10:05 AM	**Session 14:** Unusual Interconnects and Other Uses for Light
8:00 AM	**Session 15:** DRAM, SRAM, and Non-Volatile Memories
8:00 AM	**Session 16:** Energy Harvesting, Piezo and Chargers
1:30 PM	**Session 17:** Highlighted Chip Releases for AI
3:35 PM	**Session 18:** Technology and Circuits for Domain-Specific Accelerators
1:30 PM	**Session 19:** High-Voltage, Isolated and Display Power
1:30 PM	**Session 20:** RF Transceiver Subsystems from cm-Wave to THz
1:30 PM	**Session 21:** Sensor Interfaces
1:30 PM	**Session 22:** Circuits in Extreme Environments
3:35 PM	**Session 23:** Next-Generation Optical Transceivers
3:35 PM	**Session 24:** Displays

9:30 AM to 1:30 PM – Book Displays
9:30 AM to 1:30 PM – Corporations/Institution Exhibition
3:00 PM to 8:00 PM – Book Displays
3:00 PM to 8:00 PM – Corporations/Institution Exhibition
5:00 PM to 7:00 PM – Demonstration Session
5:30 PM – Author Interviews • Social Hour

ISSCC 2026 SCHEDULE OF EVENTS

Events Below are Included with your Conference Registration

ISSCC 2026 • Tuesday, February 17th

Evening Events

8:00 PM

EE2: Generative AI for Silicon Design: Mastering Complexity, Democratizing Design, and Building Trust

EE3: The Augmented Human - Will Chips in Our Brain Enhance Our Cognitive Abilities?

ISSCC 2026 • Wednesday, February 18th Paper Sessions

8:00 AM	**Session 25:** Hardware Security
8:00 AM	**Session 26:** Compute Power and Supply Modulators
8:00 AM	**Session 27:** Frequency Generators, Multipliers and Modulators
8:00 AM	**Session 28:** Innovations from Outside the (ISSCC) Box
10:05 AM	**Session 29:** Biochemical Sensors for Life Sciences and Agriculture
8:00 AM	**Session 30:** Compute-in-Memory
1:30 PM	**Session 31:** AI Accelerators
1:30 PM	**Session 32:** Low-Power Noise-Shaping ADCs
3:35 PM	**Session 33:** Time-Varying Circuit Techniques from RF to mm-Wave
1:30 PM	**Session 34:** Integrated Radar and UWB Transceivers from Microwave to Sub-THz
3:35 PM	**Session 35:** Low Power Wireless Transceivers for Localization and Communications
1:30 PM	**Session 36:** Neural and Biomedical Interfaces
1:30 PM	**Session 37:** Memory Interface
	5:30 PM – Author Interviews

Optional Educational Events

ISSCC 2026 • Thursday, February 19th

Forums

8:00 AM

F3: Powering the Future of AI, HPC, and Chiplet Architectures: From Dies to Package and Rack

F4: The Race for 6G FR3 (7-24GHz): From Network Deployment to System Integration and Breakthrough Technology

F5: Analog for AI and AI for Analog: What the Analog/RF People Can Do and Leverage in the AI Era

F6: Calibration and Dynamic Matching Techniques for High-Performance Data Converters

Short Course

8:00 AM

SC: Circuits for Optical Subsystems: Communications and Beyond

ISSCC 2026 Circuit Insights

(Saturday, Feb. 14, 2026, 8:45 AM – 6:00 PM)

Organizer/Moderator:
Ali Sheikholeslami, *University of Toronto, Toronto, Canada*
ISSCC Education Chair

ISSCC 2026 offers the fifth edition of its Circuit Insights on Saturday, Feb. 14, 2026, 8:45am - 6:00pm PST. As in the past four years, this event targets 3rd- and 4th-year undergraduate students and starting graduate students in the field of circuit design, but may also be of interest to new circuit design engineers. The event will be held in person for a small audience of 50 students (by invitation only) at the ISSCC venue at the Marriott Hotel in San Francisco, and will be recorded for later release on the SSCS/ISSCC YouTube channel.

This event consists of an Industry Perspective followed by four 50-minute talks on some of the fundamental aspects of circuit design. There will be a 10-minute interactive Q&A Session at the end of each talk.

Tentative Agenda

Time	Topic
8:45 AM	Coffee
9:15 AM	**Welcoming Remarks** **Edith Beigné,** *ISSCC Conference Chair* **Daniel Friedman,** *SSCS President*
9:30 AM	**Semiconductor Innovation -** **The Smallest Devices for the Greatest Impact** **Myung-Hee Na,** *VP and General Manager, Technology Research, Intel*
10:40 AM	Break
11:00 AM	**Device Physics Fundamentals for Circuit Designers** **Ali Sheikholeslami,** *University of Toronto, Toronto, Canada*
12:00 PM	Networking Lunch
1:00 PM	**MOS Transistor Modeling Using the Inversion CoePicient** **Christian Enz,** *EPFL, Switzerland*
2:00 PM	**CMOS Transistor Sizing: Gm/ID Approach** **Boris Murmann,** *University of Hawaii at Manoa, Hawaii*
3:00 PM	Break
3:30 PM	**Voltage and Current Reference Generation** **Shanthi Pavan,** *IIT Madras, India*
4:30 PM	**Panel Discussion** (with all the Speakers)
4:50 PM	Attendees' Feedback/Quiz, Group Photo
5:00 PM	Ice Cream and Networking (with Speakers, SRP attendees, ISSCC ITPC Members)
6:00 PM	Conclusion

TUTORIALS

There are a total of 10 tutorials this year on 10 different topics. Each tutorial, selected through a competitive process within each subcommittee of the ISSCC, presents the basic concepts and working principles of a single topic. These tutorials are intended for non-experts, graduate students and practicing engineers who wish to explore and understand a new topic.

Sudip Shekhar
ISSCC Tutorials Chair

8:30 AM
T1: Fundamentals of Energy-Efficient LDO Regulator Designs

Hyun-Sik Kim
KAIST, Daejeon, Korea

Low-dropout (LDO) regulators are essential for providing stable, ripple-free power with a compact footprint. However, the unavoidable dropout voltage required to maintain adequate regulation performance results in significant power loss, often causing LDO regulators to be perceived as inefficient powe-management elements. This tutorial investigates the fundamental trade-off between dropout voltage and regulator performance by exploring the operational principles and analytical frameworks governing this relationship. We discuss advanced design strategies that effectively overcome this traditional trade-off, enabling extremely low dropout voltages without compromising critical performance metrics. Additionally, we examine design techniques aimed at achieving ultra-low quiescent current consumption. The tutorial concludes by comparatively discussing the strengths and limitations of various state-of-the-art, energy-efficient LDO topologies.

Hyun-Sik Kim is an Associate Professor at KAIST, Daejeon, Korea. He received his Ph.D. degree in electrical engineering from KAIST in 2014. His research interests include analog integrated circuit design, with a particular focus on display drivers and power-management circuits. He has authored or co-authored 90+ peer-reviewed journal and conference papers, including 19 JSSC papers, 20 ISSCC papers, 17 VLSI Symposium papers, and 6 CICC papers. He served as a Guest Editor for IEEE SSC-L and IEEE JESTPE, and is currently serving as a Technical Program Committee (TPC) member for IEEE ISSCC and A-SSCC. Prof. Kim was Chair of the Power Management Technical Subcommittee for IEEE CICC, was Program Chair for PwrSoC 2025, and has been appointed as an IEEE SSCS Distinguished Lecturer (DL) for the term 2024–2026.

8:30 AM
T2: Fundamentals of Cryptography for Chip Designers: Classical to Post-Quantum

Thomas Pöppelmann
Infineon Technologies, Neubiberg, Germany

The advent of quantum computers poses a significant threat to digital communication systems. Now that the NIST post-quantum cryptography (PQC) standardization process has concluded, support for PQC is needed not only in high-end security systems but also in general purpose devices. During this tutorial we discuss how state-of-the-art classical cryptography works today and introduce the basics of PQC. We describe challenges faced by chip architects and IC designers when adding support for the new cryptographic schemes in silicon devices. Additionally, we examine techniques for secured implementation of PQC and how PQC might drive requirements for larger memories and faster communication interfaces in constrained devices like embedded microcontrollers.

Thomas Pöppelmann is a Senior Principal Engineer at Infineon Technologies AG. He is leading the Security Innovation team and working as Platform Security Architect for MCU, IoT, and Automotive. His main area of work is the definition of security architectures and the development of concepts for secured cryptographic modules, security standardization, and innovation projects. His research interests are security architecture, physical protection of cryptographic implementations, post-quantum cryptography, and practical lattice-based cryptography. In 2015 he obtained his PhD (Dr.-Ing.) on practical lattice-based cryptography under the supervision of Prof. Dr.-Ing. Tim Güneysu at Ruhr-University Bochum.

8:30 AM

T3: Design Techniques for Robust and Energy-Efficient Biomedical Readouts

Taekwang Jang
ETH Zurich, Zurich, Switzerland

As wearable and implantable electronics typically operate under stringent energy constraints, their energy efficiency is a primary concern. At the same time, ensuring reliable and robust acquisition of small signals in the presence of various types of noise and interference is essential. In this tutorial, I will introduce the fundamentals and recent design techniques of analog and mixed-signal circuits for energy-constrained biomedical interface systems.

Taekwang Jang received his B.S. and M.S. in EE from KAIST, and Ph.D. from the University of Michigan. In 2008-2013, he worked at Samsung Electronics. Currently, he is an associate professor at ETH Zurich and is leading the Energy-Efficient Circuits and Intelligent Systems group.

He focuses on circuits and systems for energy-constrained applications. Essential components such as an analog interface, energy harvester, PLL, and power/data converters are his primary interests. He received the SSCS New Frontier Award and ISSCC Jan Van Vessem Award for Outstanding European Paper. He is a TPC for the ISSCC, an AE for the JSSC, and an SSCS DL.

10:30 AM

T4: Fundamentals of Compute-in-Memory: From Circuits to Systems

Jaydeep Kulkarni
The University of Texas at Austin, Austin, TX

Compute-in-memory (CIM) designs are being actively researched to address the “Memory Wall” bottleneck in modern computing systems. This tutorial will begin by discussing system design considerations to tackle data-movement challenges with CIM, then focus on the core principles for performing arithmetic and logic computations using both analog and digital approaches. The design trade-offs, prospects, and challenges of future CIM applications will also be covered.

Jaydeep Kulkarni is an associate professor and a fellow of the Silicon Labs endowed chair at the University of Texas at Austin. His research focuses broadly on IC design. He has been a distinguished lecturer for IEEE SSCS, CAS, and ED societies and a TPC/AE at various conferences and journals.

10:30 AM

T5: Fundamentals of Image Sensors: From Photon to Image

Min-Woong Seo
Samsung Electronics, Hwaseong, Korea

This tutorial introduces the main signal path of an image sensor, from light capture to readout, conversion, and image output. It highlights how design choices impact performance, using examples such as rolling vs. global shutter architectures and column vs. pixel-parallel ADCs. The session balances technical depth with broader context, aiming to engage not only image sensor specialists and enthusiasts but also engineers from other integrated circuit fields. By connecting fundamental concepts to practical design considerations, the tutorial provides a clear perspective on how sensor architecture influences system behavior and imaging outcomes.

Min-Woong Seo received his Ph.D. degree from Shizuoka University, Hamamatsu, Japan, in 2012, with a dissertation focused on low-noise, HDR CMOS image sensors using high-performance ADCs. In 2018, he joined the Semiconductor R&D Center (SRDC) at Samsung Electronics, Hwaseong, Korea. He has been serving on the TPC of EI since 2018 and of the ISSCC since 2024. He has also been a steering committee member of the Korean Image Sensor Society (KISS) since 2024, a board member of the International Image Sensor Society (IISS) since 2025, and an advisory board member of Image Sensors (IS) Asia since 2025.

10:30 AM

T6: Principles and Practices of High-Speed Digital-to-Analog Converter Design

Shiyu Su
University of Waterloo, Waterloo, Canada

High-speed DACs (>GS/s) are crucial not only as performance-limiting building blocks for wideband ADCs but also as key enablers for various emerging communication and computing systems, such as software-defined/DSP-based transceivers and quantum computers. This tutorial offers a comprehensive introduction to the design of high-speed DACs, beginning with system context and fundamental concepts, and progressing to architectural and circuit-level design trade-offs. Additionally, we will delve into advanced techniques for enhancing bandwidth and linearity, including time/frequency interleaving, operation in higher Nyquist zones, mismatch error shaping/mapping/scrambling, and digital predistortion. Finally, we will cover essential layout techniques and strategies.

Shiyu Su is currently an Assistant Professor at the University of Waterloo. He received his Ph.D. degree from the University of Southern California. He is a Senior Member of the IEEE and serves as a Technical Program Committee Member for ISSCC and DAC. He was the recipient of the IEEE SSCS Predoctoral Achievement Award for 2017–2018 and a co-recipient of the Best Student Paper Award (First Place) at the RFIC 2022. He was also a Ming Hsieh Institute Scholar from 2019 to 2020.

1:30 PM

T7: Embedded Memory and Logic Circuit Design in Technologies Beyond FinFET

Zheng Guo
Intel, Portland, OR

With the advent of Gate-All-Around (GAA) technologies, the discretization of transistor width known to FinFET technologies is no longer required. This enables additional flexibility to optimize embedded memory and logic designs through extensive DTCO. Furthermore, power supply from the backside is becoming available and opens additional design-optimization opportunities. This tutorial will focus on the opportunities and challenges in embedded memory and logic circuit design in technologies beyond FinFET.

Zheng Guo received his B.S. degree in Computer Engineering from UIUC in 2003, and M.S. and Ph.D. degrees in electrical engineering from the UC Berkeley in 2005 and 2009, respectively. He joined Intel in 2010, where he is currently a Sr. Principal Engineer and leads embedded-memory-technology/design pathfinding and development.

1:30 PM

T8: Interference Mitigation Techniques in Wireless Communication Systems

Negar Reiskarimian
Massachusetts Institute of Technology, Cambridge, MA

The pursuit of ubiquitous connectivity and the evolution of wireless communication technologies such as 5G and beyond and IoT have increased the number of connected devices rapidly and have spurred a growing demand for front-end designs that can operate across a wide frequency spectrum for various communication standards. Furthermore, the growing number of devices creates increasing interference in the environment, from unknown in-band and out-of-band blockers to self-interference in full-duplex and radar systems, and spatial blockers in phased-array and MIMO systems. In this tutorial, a review of circuit and system design techniques for mitigating various types of interference is presented and state-of-the-art performance is summarized.

Negar Reiskarimian received the B.S. and M.S. degrees in electrical engineering from Sharif University of Technology, Iran, in 2011 and 2013, and the M.Phil. and Ph.D. degrees in electrical engineering from Columbia University, New York, NY, USA, in 2017 and 2020. She is currently an Associate Professor with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, USA. Her research interests include RF and millimeter-wave circuits and systems for a variety of applications. She is currently serving on the TPCs of ISSCC, RFIC and IMS. She was co-recipient of several awards, including the ISSCC 2024 Jack Kilby Outstanding Student Paper Award and 2024 RFIC Best Student Paper Award (1st place).

3:30 PM

T9: Clocking and CDR Techniques for High-Performance Wireline Transceiver

Wei-Zen Chen
National Yang Ming Chiao Tung University, Hsinchu, Taiwan

This tutorial will begin with an overview of jitter budgets for high-performance, DSP-based transceivers, followed by an introduction to the design of high-precision clock generators and CDR circuits. Topics will include low-noise phase-locked loops (PLLs), clock distribution networks, and calibration techniques for clocks and time-interleaved analog-to-digital converters (ADCs). The tutorial will also highlight recent advancements on baud-rate phase detectors and cooperative techniques between CDR and equalizers.

Wei-Zen Chen (M'00–SM'11) is a professor at the Institute of Electronics and the Department of Electronics and Electrical Engineering at National Yang Ming Chiao Tung University (NYCU). He has served as an Associate Editor of IEEE Solid-State Circuits Letters, a Guest Editor of the IEEE JSSC, IEEE OJ-SSCS, and a Technical Program Committee (TPC) member for the IEEE Asian Solid-State Circuits Conference (A-SSCC) and the IEEE Custom Integrated Circuits Conference (CICC). Currently, he is the APAC Chair of the ISSCC regional committee. Professor Chen has published over 100 peer-reviewed journal and conference papers. His research interests include mixed-signal integrated circuits for wireless and wireline communication systems, with a focus on high-speed interconnects, optical communication, and radar sensing systems

3:30 PM

T10: Doherty Power Amplifier: Fundamentals and Recent Advances

Taiyun Chi
Rice University, Houston, TX

Doherty PA architecture has gained growing interest due to its superior efficiency when amplifying modulated signals. This tutorial will begin with Doherty PA fundamentals, along with a few intuitive insights often overlooked in textbooks and research articles. We will then highlight several key ingredients in achieving first-pass Doherty PA design success. Finally, we will delve into recent demonstrations featuring bandwidth extension, deep back-off efficiency enhancement, and size reduction.

Taiyun Chi is an Associate Professor at Rice University. His group received the 2024 ISSCC Lewis Winner Outstanding Paper Award, 2021 CICC Best Student Paper Award, and multiple Best Paper Award Finalists at IMS (2024, 2021) and RFIC (2023, 2022). He was also a recipient of the NSF CAREER Award.

Power Efficient Circuits and Systems for Next-Gen Agentic AI and Robotics

Organizers: **Jun-Seok Park,** *S.LSI, Samsung Electronics, Hwaseong, Korea*
Frank Prämaßing, *Infineon Technologies Austria AG, Villach, Austria*

Co-Organizers: **Patrik Arno,** *STMicroelectronics, Grenoble, France*
Mahmut Ersin Sinangil, *Nvidia, Santa Clara, CA*
Eric Wang, *TSMC, Hsinchu, Taiwan*
Sugako Otani, *Renesas Electronics, Tokyo, Japan*
Santosh Ghosh, *Nvidia, Hillsboro, OR*

Champions: **Tanay Karnik,** *Intel, Hillsboro, OR*
Makoto Ikeda, *University of Tokyo, Tokyo, Japan*

The evolution of AI is now moving toward a new frontier—Agentic AI and Physical AI. Agentic AI represents a shift toward goal-directed, autonomous behavior, while Physical AI refers to embodied systems that interact directly with the physical world. Accordingly, emerging trends in robotics are revolutionizing industrial automation, digitalization, and sustainability.This shift is not merely a transformation in software paradigms but also demands fundamental innovations in hardware design and semiconductor architecture. Real-time computation for agent-based systems, memory-compute integration, and interfaces between sensors, actuators, and edge computing are becoming critical areas that pose new challenges and opportunities for next-generation chip design.This is a forum to hear expert opinions on the crucial aspects of robotics and on the efforts and breakthroughs at the cutting edge of the industry from a circuit and system perspective. We discuss a comprehensive trend of pioneering architectures, systems, and circuits designed to address the power-performance efficiency challenges associated with Agentic and Physical AI.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Jun-Seok Park,** *S.LSI, Samsung Electronics, Hwaseong, Korea*
8:25 AM	**Robotics and Physical AI: The Next Frontier** **Kamesh Medepalli,** *Infineon, San Jose, CA*
9:15 AM	**From VLSI Through Algorithms: Optimizing the Computing Stack for Agentic AI** **Brucek Khailany,** *NVIDIA, Austin, TX*
10:05 AM	Break
10:20 AM	**Agentic AI on Mobile Devices** **C. L. Chang,** *MediaTek, Hsinchu, Taiwan*
11:10 AM	**Revolutionizing Long-Term Memory in AI: New Horizons with High-Capacity and High-Speed Storage** **Jun Deguchi,** *Kioxia, Yokohama, Japan*
12:00 PM	Lunch
1:20 PM	**Architecting Silicon for Intelligence and Autonomy in Embodied AI** **Arijit Raychowdhury,** *Georgia Institute of Technology, Atlanta, GA*
2:10 PM	**High-Performance DC-DC Conversion for Next-Gen Computing: From Cloud to Edge** **Wanyuan Qu,** *School of Integrated Circuits, Zhejiang University, Hangzhou, China*
3:00 PM	Break
3:15 PM	**On the Move - Semiconductor Technologies for Motion Control in Humanoid Robotics** **Mark Muenzer,** *Infineon, Munich, Germany*
4:05 PM	**Hardware Security Challenges for Agentic AI** **Ingrid Verbauwhede,** *KU Leuven, Leuven Belgium*
4:55 PM	Closing Remarks

Electrical and Optical Links Towards 400G+ Connectivity

Organizers: **Masum Hossain,** *Carleton University, Ottawa, Canada*
Tamer Ali, *Mediatek, Irvine, CA*

Co-Organizers: **Kenny Hsieh,** *TSMC, Hsinchu, Taiwan*
Jay Im, *AMD, San Jose, CA*

Champions: **Wei-Zen Chen,** *National Yang Ming Chiao Tung University, Hsinchu, Taiwan*
Bill Redman-White, *Top-IC, Southampton, United Kingdom*

This forum aims to bring the latest developments towards achieving high bandwidth density through electrical and optical connectivity. The forum will include standards, state-of-the-art electrical and optical solutions and applications. The forum will also present the development of the technology platforms by foundries to showcase their latest photonic technology and packaging solutions.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Masum Hossain,** *Carleton University, Ottawa, Canada*
8:25 AM	**Data Centre Interconnect: 400G, 800G, and Terabit Pluggable Optics** **Andy Bechtolsheim,** *Arista, Santa Clara, CA*
9:15 AM	**Analog and Mixed-Signal Approaches for Low-Complexity Coherent Optical Links** **Pavan Kumar Hanumolu,** *University of Illinois (UIUC), Urbana, IL*
10:05 AM	Break
10:20 AM	**State-of-the-Art 224+ Gb/s Electrical-Optical Interconnect** **Ehung Chen,** *MediaTek, Hsinchu, Taiwan*
11:10 AM	**Latency-Optimized Silicon Photonic I/O** **Ganesh Balamurugan,** *Celestial AI, Santa Clara, CA*
12:00 PM	Lunch
1:20 PM	**Emerging Low-Latency Optical Connectivity** **Nikola Nedovic,** *Nvidia, Santa Clara, CA*
2:10 PM	**400 Gb/s Coherent Optics** **Xin Yin,** *IMEC, Leuven, Belgium*
3:00 PM	Break
3:15 PM	**Scaling AI with Light: 3D Photonic Solutions for Next-Gen Connectivity** **Ritesh Jain,** *Lightmatter, Mountain View, CA*
4:05 PM	**Silicon Photonics Platform for Next-Generation Data Communication Technologies** **Chih-Tsung Shih,** *TSMC, Hsinchu, Taiwan*
4:55 PM	Closing Remarks

Morning Session:
Next Generation Circuit Designer 2026 Workshop

Co-Chair: **Mondira Pant,** *Intel, Santa Clara, CA*
Co-Chair: **Wanghua Wu,** *Samsung, San Jose, CA*
Student Lead: **Elpida Karapepera,** *University of Washington, Seattle, WA*

Workshop Committee:

Aishwarya Natarajan, *Hewlett Packard Labs, Palo Alto, CA*
Alana Dee, *University of Washington, Seattle, WA*
Ben Keller, *Nvidia, Santa Clara, CA*
Dilara Caygara, *Boston University, Boston MA*
Emily Naviasky, *IBM, Yorktown Heights, NY*
Jiamin Li, *SUSTech, University of Shenzhen, China*
Kamala Raghavan Sadagopan, *Qualcomm, San Diego, CA*
Kwantae Kim, *Aalto University, Espoo Finland*
Marziyeh Rezaei, *University of Washington, Seattle, WA*
Najme Ebrahimi, *Northeastern University, Boston, MA*
Shanshan Xie, *Intel, Austin, TX*
Sukanya S Meher, *Synopsys, Sunnyvale, CA*
Yingying Fan, *Washington University, St. Louis, MS*
Yu-Chi Lin, *UC Berkeley, CA*

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Kathy Wilcox, *AMD, Boxborough MA*
Farhana Sheikh, *Intel, Hillsboro, OR*
Zeynep Deniz, *IBM Research, Yorktown Heights, NY*

The IEEE SSCS Women in Circuits together with ISSCC will be co-sponsoring the "Next Generation Circuit Designer 2026" for young professionals and students. This is a an educational workshop for a diverse set of graduate and undergraduate students, and young professionals who have graduated with a B.S/M.S. within the last two years, who are interested in learning how to excel at academic and industry careers in computer science and computer and electrical engineering.

The panel on "*Chip In for Change: Career Insights for Young Designers in an AI-First, Eco-Conscious World*", with panelists from diverse regions, backgrounds and career levels, will touch upon topics such as:

- networking and mentoring; choosing or changing a career path, a research topic, or an advisor;
- time management, work-life balance, and mental and physical well-being;
- managing day-to-day life in both graduate school and industry;
- dealing with challenges and conflict, and more.

The panelists are:

Sashi Oilisetty, *Executive Director, Synopsys, USA*
Carolina Mora Lopez, *Scientific Director, imec, Belgium*
Pei-Yun Tsai, Professor, *National Taiwan University, Taiwan*
Srabanti Chowdhury, *Professor, Stanford University, USA*

Bingo Networking Event
(Open to all Attendees)
4:00 - 6:00 PM

Women in Circuits (WiC) together with ISSCC will be holding a networking and mentoring session on Sunday afternoon. Distinguished panelists from the career panel, WiC members, and other participants will play getting-to-know-you bingo to promote engagement between various members of the community. This will give participants the chance to network and mingle with people across a spectrum of seniority in the field in a casual setting.

EE1: Student Research Preview (SRP) 8:00 PM

The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of 26 sixty-second presentations followed by a Poster Session by graduate students from around the world, which have been selected on the basis of a short submission concerning their ongoing research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in three theme sections: 1) RF, mmWave TRX, 2) ML/AI/Security, and 3) Power, Wireline and Sensing.

The SRP will include an inspirational lecture by Dr. Kinam Kim, Senior Advisor and Former CEO, Samsung Electronics. The SRP begins at 8:00 pm on Sunday, February 15th. It is open to all ISSCC registrants.

SRP Organizing Committee

Co-Chair:	**Jerald Yoo**, *Seoul National University, Korea*
Co-Chair:	**Mondira (Mandy) Pant**, *Intel, MA*
Advisor:	**Anantha Chandrakasan**, *Massachusetts Institute of Technology, MA*
Advisor:	**Jan Van der Spiegel**, *University of Pennsylvania, Philadelphia, PA*
Media/Publications:	**Laura Fujino**, *University of Toronto, Toronto, Canada*
A/V:	**Trudy Stetzler**, *Halliburton, Houston, TX*

Committee Members

Utsav Banerjee
IISC, India

Woo-Seok Choi
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Zeynep Deniz
IBM Research, NY

Sijun Du
Delft University of Technology, The Netherlands

Philex Fan
National Cheng Kung University, Taiwan

Pasqualina Fragneto
ST Microelectronics, Italy

Antoine Frappé
University of Lille, France

Hao Gao
Southeast University, China.

Preet Garcha
Texas Instruments, TX

Bongjin Kim
KAIST, Korea

Jaydeep Kulkarni
University of Texas at Austin, TX

Matthias Kuhl
University of Freiburg, Germany

Hyunjoo Jenny Lee
KAIST, Korea

Kyuho Jason Lee
Yonsei University, Korea

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Nvidia, CA

Takuji Miki
Kobe University, Japan

Noriyuki Miura
Osaka University, Japan

Phillip Nadeau
Analog Devices, MA

Mondira Pant
Intel, MA

Chutham Sawigun
imec, Belgium

Filip Tavernier
KU Leuven, Belgium

Pei-Yun Tsai
National Taiwan University

Rabia Tugce Yazicigil
Boston University, MA

Jerald Yoo
Seoul National University, Korea

Lian Zhang
Apple, CA

Plenary Session — Invited Papers

Chair: **Edith Beigné,** *Meta, Menlo Park, CA*
ISSCC Conference Chair

Associate Chair: **Keith Bowman,** *Qualcomm, Raleigh, NC*
ISSCC International Technical-Program Chair

FORMAL OPENING OF THE CONFERENCE **8:30 AM**

1.1 Advancing Horizons for AI: Perspectives on Semiconductor Innovations — 8:50 AM

Rick Tsai, *Vice Chairman and CEO, MediaTek, Hsinchu, Taiwan*

AI is redefining the semiconductor landscape. Exponential growth in compute, bandwidth, and power efficiency is driving the proliferation of agentic and physical AI. The paradigm is shifting from performance alone to breakthroughs in scalable and energy-efficient architectures and cross-layer system innovation with close cooperation across silicon, design, heterogeneous hardware integration, and software. This plenary explores the key vectors of advanced packaging, power delivery, thermal management, high-bandwidth memory, interconnects, and wireless communication that will shape increasingly intelligent, robust AI systems for the decade ahead.

1.2 Quantum Computing – Toward Large-Scale Fault-Tolerant Quantum Computing — 9:20 AM

Heike Riel, *IBM Fellow and Head of Science of Quantum & Information Technologies, IBM Research, Rüschlikon, Switzerland*

Quantum computing is advancing rapidly, offering the potential to transform computational paradigms and tackle problems that are intractable for classical systems. Realizing practical quantum systems demands the development of an entirely new computing stack—from qubits and quantum processors to components, wiring and control electronics, transpilers, error handling, software, algorithms, and the compute architecture to integrate quantum and classical resources at scale.

This plenary will provide an overview of the current state of quantum computing and outline the milestones on the path toward building a large-scale, fault-tolerant quantum computer by 2029. The significant improvements in hardware, software, and system integration, pushing the performance of quantum computing to reach quantum utility and advance toward quantum advantage, will be presented. Breakthroughs in error correction and a modular approach indicated in the IBM Quantum Roadmap outline a clear path to quantum systems using 200 logical qubits and 100 million quantum operations by 2029 and 2,000 logical qubits a few years later. Furthermore, advances in quantum algorithms, combined with the integration of quantum systems and high-performance computing (HPC), will unlock powerful synergies—accelerating the timeline for applications previously considered to be far in the future.

ISSCC, SSCS, IEEE AWARD PRESENTATIONS **9:50 AM**

BREAK **10:15 AM**

1.3 Powering the AI Supercycle: Design for AI and AI for Design — 10:45 AM

Anirudh Devgan, *President and CEO, Cadence, San Jose, CA*

The AI supercycle is rapidly increasing demand for compute performance and scalability across all levels, from data centers to edge devices. By 2030, the semiconductor total addressable market (TAM) is projected to reach $1.2T with electronic systems at $5.2T. With silicon designs surpassing 200 billion transistors and chiplet-based architectures becoming common, traditional electronic-design-automation (EDA) workflows are insufficient. This plenary discusses how agentic AI can be applied to complex silicon and system design tasks through multi-agent orchestration and iterative reasoning, outlining a framework for its use in EDA solutions, highlighting some of the challenges, and exploring future directions. From optimizing power, performance, and area of silicon to managing data centers, AI-powered solutions are critical for the engineers designing the next generation of AI infrastructure.

1.4 Empowering the Next Wave of Silicon Engineers — 11:15 AM

Hope Giles, *Vice President, Hardware Technologies, Apple, Cupertino, CA*

Developing custom chips for specific applications enables fundamentally better products. As part of a full-stack optimization approach to product design, application-specific systems on chip (SoCs) have been one of the keys to delivering game-changing performance, power efficiency, capabilities, and user experiences. This plenary provides examples of how custom silicon makes delivering innovative breakthroughs in products possible and how techniques like design modularity help manage the SoC scaling challenge. As emerging applications, including artificial intelligence (AI), transform both silicon demand and our design methodologies, we need to reimagine how we motivate and educate the next generation of silicon engineers to address these challenges. We will share our experiences in industry/university/student interactions and how the industry can revitalize these programs. The future of custom silicon depends on all of us investing in the next wave of engineers who will create tomorrow's innovative products.

PRESENTATION TO PLENARY SPEAKERS — 11:45 AM

CONCLUSION — 11:50 AM

SESSION 2

Processors

Session Chair: Mark Anders, *Intel , Hillsboro, OR*
Session Co-Chair: Francesco Conti, *University of Bologna, Bologna, Italy*

1:30 PM

2.1 AMD Instinct MI350 Series GPUs: CDNA 4-Based 3D-Stacked 3nm XCDs and 6nm IODs for AI applications

R. Adaikkalavan[1], A. Smith[1], T. Singh[1], S. Rangarajan[1], E. Chapman[1], S. Naffziger[2], S. Maiyuran[3], C. Chen[4], S. Sundaram[1], M. Silla[1], D. Law[5], K. Hoover[1], S. Lipson[1], K. Duda[2], V. Parthasarathy[6], D. John[1], H. Vemulapalli[1], S. P. K. Gade[7]

[1]AMD, Austin, TX; [2]AMD, Fort Collins, CO; [3]AMD, Folsom, CA
[4]AMD, Shanghai, China; [5]AMD, Markham, Canada; [6]AMD, San Diego, CA
[7]AMD, Hyderabad, India

1:55 PM

2.2 DS1 A Quad-Chiplet AI SoC with Full-Chip Scalable Mesh Over 16Gb/s UCIe-Advanced Die-to-Die Interface for Large-Scale AI Inferencing

C-H. Yu, J. Bae, J. Kim, H. Kim, W. Shin, J-S. Yoon, Y-J. Jin, J. Oh, J. Lee, E. Kim, M. Chi, S. Choi, D. Kim, H. Jo, H. Kim, H. Heo, H. Kim, S-G. Kim, M. Choi, S. Je, J. Ham, J. Yoon, Y. F. Arthanto, S-I. Bae, S. Park, J. Lee, H. Chae, K. Ryu, Y. Kim, J-O. Seo, N. Cho, T. Jeon, G. Ahn, M. Ki, J. Choi, S. Baek, D. Kim, J. Kim, S. Kang, S. Son, M. Kim, Y. Choe, Y. Lee, S. Park, J. Oh

Rebellions, Seongnam, Korea

2:20 PM

2.3 DS1 A 71.3mJ/Frame End-to-End Driving Processor with Flexible Heterogeneous Core Orchestration via Sparsity Reasoning

J. Jung[1,2], S. Lee*[1], J. Yoo[2], G. Yun[2], K. J. Lee[2]*

[1]Ulsan National Institute of Science and Technology, Ulsan, Korea
[2]Yonsei University, Seoul, Korea
*Equally Credited Authors (ECAs)

2:45 PM

2.4 UniC-Vision: A 14.4Gb/s 7.3pJ/b Universal Vision Transformer OFDM Channel Estimation Accelerator for B5G/6G AI-RAN

S. Yun[1,2], C. Lee[1,2], S. Kwon[1], J. Chang[3], Z. Zhang[3], Y. Lee[1]

[1]Korea Advanced Institute of Science and Technology, Daejeon, Korea
[2]Pohang University of Science and Technology, Pohang, Korea
[3]University of Michigan, Ann Arbor, MI

3:00 PM

2.5 A 1.1mm², 14.4ns, 13.1pJ/b Forward Error Correction with Ordered-Statistics Post Processing for Ultra-Reliable and Low-Latency Communications

C-H. Lu[1], W. Tang[1], J. Kim[2], Y. Lee[3], Z. Zhang[1]

[1]University of Michigan, Ann Arbor, MI
[2]Pohang University of Science and Technology, Pohang, Korea
[3]Korea Advanced Institute of Science and Technology, Daejeon, Korea

Break 3:15 PM

3:35 PM

2.6 Spyre: An Inference-Optimized Scalable AI Accelerator for Enterprise Workloads

M. Cohen[1], M. Kar[1], S. Venkataramani[1], V. Srinivasan[1], B. Veraa[2], M. Ziegler[1], N. Cao[1], A. Ranjan[1], J. Silberman[1], M. Guillorn[1], S. Woodward[3], J. Lancaster[1], J. Hursey[4], K-H. Kim[1], A. Mannari[5], A. Nagarajan[1], A. Samajdar[1], B. Hekmatshoartabari[1], B. Galbraith[3], C. Zhou[1], D. Satterfield[1], G. Still[6], G. Tellez[1], I. Nair[1], I. Masilamanai[2], J. Jung[1], K. Randhawa[2], M. Schaal[1], M. Lutz[1], P. Crumley[1], P. Jacob[1], P. Chatarasi[1], R. Jain[1], S. Lee[1], S. Sen[1], S. Krithivasan[1], S. Rider[1], S. Jain[1], S. Koswatta[1], T. Roewer[1], T. Gooding[3], V. Ferrari[7], V. Zalani[1], Z. Ren[1], K. Reick[2], L. Maurice[8], C. Gonzalez[9], C. Catalino[2], R. Nett[2], P-F. Lu[1], R. Senger[1], L. Chang[1]

[1]IBM Research, Yorktown Heights, NY; [2]IBM Infrastructure, Austin, TX
[3]IBM Infrastructure, Rochester, MN; [4]IBM Research, Rochester, MN
[5]IBM Research, Zurich, Switzerland
[6]IBM Infrastructure, Research Triangle Park, NC
[7]IBM Research, Sao Paulo, Brazil; [8]IBM Research, Austin, TX
[9]IBM Infrastructure, Yorktown Heights, NY

4:00 PM

2.7 DS2 Tiamat: A 98-to-134ms/Step Transformer-Based Diffusion Model Processor Supporting Classifier-Free Guidance for Image Generation

P-Y. Lu, P-W. Chen, S-H. Yeh, Z-J. Zhang, Y-T. Chen, T-Y. Wang, C-T. Huang

National Tsing Hua University, Hsinchu, Taiwan

4:25 PM

2.8 MADiC: A 3nm 7.4TOPS/mm², 17.4TOPS/W Generative Diffusion Accelerator Enabled by Hardware-Compiler Co-Optimization of Memory Hierarchy and Operator Parallelism

S-W. Hsieh, Y-S. Chen, P-Y. Tsai, M-H. Lin, C-Y. Cheng, L-F. Hsu, P-H. Huang, H-W. Chih, P-H. Chiang, C-M. Chang, M-H. Chiang, C-H. Yuan, S-P. Kuo, V. Uggu, C-K. Chan, M-E. D. Shih, Y-C. Tseng, H-P. Cheng, S. Huang, C-P. Chen, S. Chang, C-M. Wang, P-Y. Yeh, J. Liu, Y-C. Chang, C-C. Ju, Y. K. Jou

MediaTek, Hsinchu, Taiwan

4:50 PM

2.9 A 0.24mJ/Frame Quadratic Interpolation 4DGS Processor with Recursive Computation Reuse and Tree-Based Parallel-Rendering

X. Yang, Y. Wang, W. Xu, Y. Qin, H. Wang, R. Guo, Z. Yue, J. Gu, S. Wei, Y. Hu, S. Yin

Tsinghua University, Beijing, China

5:15 PM

2.10 DS2 A 1286fps 0.39mJ/Frame Modeling/Rendering Unified 3D GS Processor with Locality-Optimized Computation and Reconfigurable Architecture

H. Wang, X. Feng*, W. Gao, H. Yang, Y. Liu*

Tsinghua University, Beijing, China
*Equally Credited Authors (ECAs)

Conclusion 5:30 PM

Wearable and Wireless Biomedical Systems

Session Chair: Hyung-Min Lee, *Korea University, Seoul, Korea*
Session Co-Chair: Venugopal Gopinathan, *Analog Devices, Wilmington, MA*

1:30 PM

3.1 DS1 A Multimodal Biosensing System-on-Chip with Integrated Wireless Transceiver and Power Management for Stress Monitoring

M-H. Chang[*1], *L. Chou*[*1], *Y-J. Liu*[1], *C-H. Hsu*[1], *Y-Y. Yang*[1], *B-C. Juan*[1], *G-Y. Lin*[1], *Y-J. Lin*[1], *Y-W. Huang*[1], *N. Kumar*[2], *S-P. Lin*[2], *Y-T. Liao*[1]

[1]National Yang Ming Chiao Tung University, Hsinchu, Taiwan
[2]National Chung Hsing University, Taichung, Taiwan
*Equally Credited Authors (ECAs)

1:55 PM

3.2 DS1 A Near-Field RF Reflection Transceiver ASIC for Continuous Unobtrusive Blood Pressure Monitoring

Y. Han, N. Kumar, L. Zhao, J. Y. Adebiyi, L. Jiang, H. Lu, G. Perkins, H. Tanaka, D. Akinwande, Y. Jia

University of Texas, Austin, TX

2:20 PM

3.3 DS1 A Battery-Powered Hybrid Resonant Pulse-Train Generator with Adaptive Frequency Tracking and Residual Energy Recycling for Ultrasonic Implants

X. Li[*1], *W. Peng*[*1], *L. Kumar*[1], *X. Zhao*[1], *C. Huang*[2], *S. Du*[1]

[1]Delft University of Technology, Delft, The Netherlands
[2]Iowa State University, Ames, IA
*Equally Credited Authors (ECAs)

2:45 PM

3.4 DS1 An Ultrasound-Powering TX with Standing-Wave Peak Tracking Employing Adiabatic Power Sensing Achieving 82% Power-Tracking Accuracy and <90ms Settling Time for Brain Implants

M. Gourdouparis[1,2], *C. Shi*[1], *J. Liu*[1], *Y. He*[1], *S. Stanzione*[1], *W. Serdijn*[2], *Y-H. Liu*[1]

[1]imec, Eindhoven, The Netherlands
[2]TU Delft, Delft, The Netherlands

3:00 PM

3.5 DS1 A Simultaneous Wireless Power and Full-Duplex Data Transfer System Over a Single Inductive Link Achieving 17/3.4Mb/s and 61.1% Efficiency for Miniature Biomedical Implants

T. Lu, S. Du

Delft University of Technology, Delft, The Netherlands

Break 3:15 PM

Analog Techniques & Amplifiers

Session Chair: Chinwuba Ezekwe, *Robert Bosch, Sunnyvale, CA*
Session Co-Chair: Ka-Meng Lei, *University of Macau, Taipa, Macau*

3:35 PM

4.1 A 0.64mA, -108.2dB THD+N Class-D Amplifier with Neural-Assisted Pre-Reconfiguration for Smart Power Optimization

K. Zhou, Y. Tang, Z. Shen, X. Yang, T. Qu, Y. Wang, S. Ye, Z. Hong, J. Xu
Fudan University, Shanghai, China

4:00 PM

4.2 A -102.2dB THD+N, 92% Efficiency, 1.08mW Idle Power Digital-Input Class-D Amplifier with Power-Adaptive Techniques and Dual-Edge Pulse-Width Adjustment Modulator

M. Zhang, H. Zhang, D. M. Lombardo, Q. Fan
TU Delft, Delft, The Netherlands

4:25 PM

4.3 DS2 A 0.6V 9.4μW 1,892μm² Current-Pulse-Injection Crystal Oscillator Featuring Capacitively Biased Amplifier with 242.2dBc/Hz PN FoM @1kHz Offset

H. Li[1,2], D. Shi[1], Q. Zhou[1], R. Martins[1], P-I. Mak[1], K-M. Lei[1]
[1]University of Macau, Macau, China
[2]UM Hetao IC Research Institute, Shenzhen, China

4:50 PM

4.4 A 2.1-to-3.7ppm/°C Bandgap Voltage Reference with a Current-Domain TC Compensation and ±0.06% Inaccuracy from -40°C to 125°C in 130nm CMOS

Z. Tang[1], S. Pan[2], X. Yu[3], N. N. Tan[4], Z. Zhu[1]
[1]Xidian University, Xi'an, China
[2]Tsinghua University, Beijing, China
[3]Zhejiang University, Hangzhou, China
[4]Vango Technologies, Hangzhou, China

5:05 PM

4.5 DS2 A 1ppm/°C and ±0.066% 3σ Accuracy Bandgap Reference with Temperature-Adaptive PTAT Scaling

J. Rui[1], L. Lyu[1], Y. Wan[1], K. Shan[1], W. Gu[1], C-J. R. Shi[2], X. Wu[1]
[1]East China Normal University, Shanghai, China
[2]University of Washington, Seattle, WA

5:20 PM

4.6 An Integrated Voltage and Current Reference Together Achieving 5.7 and 9.1ppm/°C from -40 to 125°C

L. Fang, Y. Zhu, R. P. Martins, C-H. Chan
University of Macau, Macau, China

Conclusion 5:35 PM

Sub-THz and mm-Wave Phased Arrays and Beamformers

Session Chair: Jose-Luis Gonzalez-Jimenez, *CEA-Leti, Grenoble, France*
Session Co-Chair: Hao Gao, *Southeast University, Nanjing, China*

1:30 PM

5.1 A Formation Flight Phased-Array Transceiver for Spatial Power Combining and Distributing Architectures in Direct-to-Device-Communication Satellite Constellations

K. Yuasa[1], Y. Takahashi[1], S. Watanabe[1], S. Kato[1], S. Ema[2], G. Hattori[2], A. Naka[3], S. Morioka[3], T. Inagawa[3], K. Murata[4], N. Honma[4], J. Mayeda[1], A. Shirane[1]

[1]Institute of Science Tokyo, Tokyo, Japan
[2]Microwave Factory, Kanagawa, Japan
[3]Interstellar Technologies, Hokkaido, Japan
[4]Iwate University, Iwate, Japan

1:55 PM

5.2 A 28GHz Frequency-Diverse Sub-Array TX with Secret Phase Keys and Antenna Subset Modulation for Eavesdropping-Resilient Wireless Communication

Q. Zhou, Y. Su, H. Guo, Y. Hu, K. Yang, T. Chi

Rice University, Houston, TX

2:20 PM

5.3 DS1 SPARTA: A Scalable, Programmable and Active mm-Wave Dual-Surface Reflect/Transmit Array with Integrated Gain and Phase Control Allowing Bidirectional Signal Routing Capability for Robust and Reconfigurable mm-Wave Networks at 60GHz

M. F. Allam[1], W. Fang*[1], Z. Shao*[1], H. Saeidi[2], A. Stepko[1], K. Sengupta[1]*

[1]Princeton University, Princeton, NJ
[2]Qualcomm, San Diego, CA
*Equally Credited Authors (ECAs)

2:45 PM

5.4 A 140GHz Full-Duplex CMOS Transceiver with Metasurface-Integrated Self-Interference-Cancelling Antenna Supporting 16Gb/s 16-QAM Dual-Mode Bidirectional Communication

J. Yang[1,2], Y. Shen[1,2], S. Xu[1], Z. Zhang[1], Z. Lin[1,2], Y. Ding[1], Y. Qian[1], J. Wan[1], Y. Cai[2], M. Zhu[1,2], S. Hu[1,2]

[1]Southeast University, Nanjing, China
[2]Purple Mountain Laboratories, Nanjing, China

Break 3:10 PM

Exploratory Receiver Architectures from GHz to THz

Session Chair: Alberto Valdes-Garcia, *IBM Research, Yorktown Heights, NY*
Session Co-Chair: Giuseppe Gramegna, *imec, Leuven, Belgium*

3:35 PM

6.1 Full-Duplex RF Canceler Achieving Wideband High-SI-Power Low-Noise Cancellation Through A Novel N-Path-Filter-Based Architecture and ML-Based Canceler Configuration

L. S. Garimella, A. Davidson, N. Patil, Y. Ma, A. Junaid, K. Pabba, H. Krishnaswamy

Columbia University, New York, NY

4:00 PM

6.2 A Phased-Array-Inspired Broadband RF Signal Processor for 2-to-32GHz Spectrum Sensing

L. Zhong, M. Tian, W. Lee

Pennsylvania State University, State College, PA

4:25 PM

6.3 A 2×2 10GS/s TTD BF Receiver Utilizing Charge-Based Summation with 10.5GHz Bandwidth and SNDR/SFDR with 49.5dB/57.5dBc in 22nm CMOS

E. Wittenhagen, D. Wilding, P. Artz, S. Linnhoff, P. Scholz, F. Gerfers

TU Berlin, Berlin, Germany

4:50 PM

6.4 A 436-to-472GHz 4-Element IF Beamforming Phased-Array Receiver in 65nm CMOS

H. Guo, H-T. Hu, Z. Lin, Z. Guo, X. Xia, K. M. Shum, C. H. Chan

City University of Hong Kong, Hong Kong, China

5:15 PM

6.5 DS2 A 26/28/37/39GHz Reconfigurable Fully Connected MIMO Receiver Front-End with On-Chip Diplexer Achieving 52-to-70dB Blocker Rejection

X. Jiang[1,2], Q. Chen*[1,2], Z. Zhang[1,2], H. Xia[2], S. Zhang[1], Y. Han[1], X. Chen[2], D. Cheng[2], L. He[2], X. Wu[1,2], L. Li[1,2], X. You[1,2]*

[1]Southeast University, Nanjing, China
[2]Purple Mountain Laboratories, Nanjing, China
*Equally Credited Authors (ECAs)

Conclusion 5:30 PM

SESSION 7

Image Sensors and Ranging

Session Chair: Augusto Ximenes, *CogniSea, Seattle, WA*
Session Co-Chair: Andreas Suess, *Google, Mountain View, CA*

1:30 PM

7.1 DS1 54×42 LiDAR 3D-Stacked System-On-Chip with On-Chip Point Cloud Processing and Hybrid On-Chip/Package-Embedded 25V Boost Generation

N. A. Dutton[1], X. Branca[2], M. Thivin[2], S. Collins[1], H. Thuaire[2], F. Martin[2], V. Clemencon[2], M. Al-Rawhani[1], D. Hall[1], A. Crocherie[1], C. Pastorelli[1], S. Taupin[2], S. Trochut[2], A. Singh[1], A. Assmann[1], B. R. Rae[1], P. Mellot[2]

[1]STMicroelectronics, Edinburgh, United Kingdom
[2]STMicroelectronics, Grenoble, France

1:55 PM

7.2 VoxCAD: A 0.82-to-81.0mW Intelligent 3D-Perception dToF SoC with Sector-Wise Voxelization and High-Density Tri-Mode eDRAM CIM Macro

H. Sang[1], Z. Wang*[1], L. He[1], G. Zhao[1], W. Xie[2], B. Wang[3], R. P. Martins[1], M-K. Law[1]*

[1]University of Macau, Macau, China; [2]KAIST, Daejeon, Korea
[3]Hamad Bin Khalifa University, Doha, Qatar
*Equally Credited Authors (ECAs)

2:20 PM

7.3 A Multi-Range, Multi-Resolution LiDAR Sensor with 2,880-Channel Modular Survival Histogramming TDC and Delay Compensation Using Double Histogram Sampling

M. Kim[1], J. Bae[1], D. Kim[1], J-H. Chun[1,2], S-J. Kim[3], J. Choi[1,2]

[1]Sungkyunkwan University, Suwon, Korea; [2]SolidVue, Seongnam, Korea
[3]Sogang University, Seoul, Korea

2:45 PM

7.4 DS1 A 480×320 CMOS LiDAR Sensor with Tapering 1-Step Histogramming TDCs and Sub-Pixel Echo Resolvers

W. Roh[1,2], C. Piao*[2], T. Jeon[1], J. Bae[1], J-H. Chun[1,2], S-J. Kim[3], J. Choi[1,2]*

[1]Sungkyunkwan University, Suwon, Korea; [2]SolidVue, Seongnam, Korea
[3]Sogang University, Seoul, Korea
*Equally Credited Authors (ECAs)

3:00 PM

7.5 A 26.0mW 30fps 400x300-pixel SWIR Ge-SPAD dToF Range Sensor with Programmable Macro-Pixels and Integrated Histogram Processing for Low-Power AR/VR Applications

M. Perenzoni[1], K. Okamoto[1,2], F. De Nisi[1], D. Perenzoni[1], J. Y. Jeong[1], Y. Zou[1], H. Mai[1], G. Quarta[1], F. P. Mattioli Della Rocca[1], Y. Okamura[1,2], D. Marani[1], M. Brian[1], D. Giorgetti[1], S. Ochiai[2], K. Tatani[2], D. Stoppa[1]

[1]Sony Semiconductor Solutions Europe, Trento, Italy
[2]Sony Semiconductor Solutions, Atsugi, Japan

Break 3:15 PM

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7.6 A 128×96 Multimodal Flash LiDAR SPAD Imager with Object Segmentation Latency of 18µs Based on Compute-Near-Sensor Ising Annealing Machine

J. Wang, T. Hong*, B. Chen*, Z. Huang, Q. Liu, M. Liu*

Fudan University, Shanghai, China
*Equally Credited Authors (ECAs)

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7.7 A Fully Reconfigurable Hybrid SPAD Vision Sensor with 134dB Dynamic Range Using Time-Coded Dual Exposures

K. Hong[1,2], J. Kang[1,2], J-H. Hwang[1,2], I. Son[3], S. Park[3], J-H. Chun[3,4], J. Choi[3,4], S-J. Kim[2]

[1]Ulsan National Institute of Science and Technology, Ulsan, Korea
[2]Sogang University, Seoul, Korea
[3]SolidVue, Seongnam, Korea
[4]Sungkyunkwan University, Suwon, Korea

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7.8 DS2 A 55nm Intelligent Vision SoC Achieving 346TOPS/W System Efficiency via Fully Analog Sensing-to-Inference Pipeline

Z. Yang[1], H. Yu[1], X. Liu[1], Z. Kong[1], H. Li[1], L. Ran[2], Z. Lyu[3], X. Feng[2], L. Zhao[3], Y. Li[1], J. Li[1], F. Zhou[1], L. Lin[1]

[1]Southern University of Science and Technology, Shenzhen, China
[2]Beijing Pixelcore Technology, Beijing, China
[3]Hefei Reliance Memory, Hefei, China

4:50 PM

7.9 A 1.09e⁻-Random-Noise 1.5µm-Pixel-Pitch 12MP Global-Shutter-Equivalent CMOS Image Sensor with 3µm Digital Pixels Using Quad-Phase-Staggered Zigzag Readout and Motion Compensation

S. Lee, S-Y. Yoo*, Y. Shim, Y-S. Choi, D. Bae, M. Ito, D. Shin, S-G. Koo, S-J. Byun, G. Cho, H. Kwon, J. Jeong, B. Kim, S-H. Han, Y. Lee, H. Sugihara, J. Jung, S. Kim, K. Lim, W. Ryu, Y. Kim, S-S. Kim, H. Shim, M-W. Seo, J-K. Lee, J. Go, J. Song*

Samsung Electronics, Hwaseong, Korea
*Equally Credited Authors (ECAs)

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7.10 DS2 A 200MP 0.61µm-Pixel-Pitch CMOS Imager with Sub-1e⁻ Readout Noise Using Interlaced-Shared Transistor Architecture and On-Chip Motion Artifact-Free HDR Synthesis for 8K Video Applications

R. Xu[1], G. Ren[2], Y. Mo[2], D. Qi[2], Q. Wang[2], S. Zhang[2]

[1]SmartSens Technology, Santa Clara, CA
[2]SmartSens Technology, Shanghai, China

Conclusion 5:30 PM

Die-to-Die and High-Speed Electrical Transceivers

Session Chair: Didem Turker Melek, *Cadence Design Systems, San Jose, CA*
Session Co-Chair: Kenny Hsieh, *TSMC, Hsinchu, Taiwan*

1:30 PM

8.1 A 48Gb/s/lane 1.24Tb/s/mm UCIe-Compliant Die-to-Die Link Over 30mm Standard Package

S. Mondal[*1], *S. Krishnamurthy*[*1], *S. Yamada*[1], *Z. Liu*[2], *J. Qiu*[1], *S. Bose*[3], *Z. Wu*[2], *G. Pasdast*[2], *J. Jaussi*[1], *M. Mansuri*[1]

[1]Intel, Hillsboro, OR; [2]Intel, Santa Clara, CA
[3]University of California, Santa Cruz, CA
*Equally Credited Authors (ECAs)

1:55 PM

8.2 A 32Gb/s 12.35Tb/s/mm² 0.36pJ/b UCIe-Like Die-to-Die Interface Featuring Edge-Triggered Transceivers in 3nm with Active LSI Packaging

W-C. Chen[1], *M-S. Lin*[1], *C-C. Tsai*[1], *S. Li*[2], *W-S. Lin*[1], *Y-J. Huang*[1], *N-C. Cheng*[1], *Y-C. Chen*[1], *W-H. Huang*[1], *C-H. Wen*[1], *H-H. Kuo*[1], *H-T. Ke*[1], *J-R. Huang*[1], *C-Y. Li*[1], *S-T. Lai*[1], *S-C. Yang*[1], *K-T. Chou*[1], *P-C. Chiou*[1], *T-H. Tsai*[1], *Y-T. Chen*[1], *Y-M. Chen*[1], *K. C-H. Hsieh*[1]

[1]TSMC, Hsinchu, Taiwan; [2]TSMC, San Jose, CA

2:20 PM

8.3 A 0.23pJ/b 24Gb/s Modular D2D Interface With Zero Wake Penalty Clock Gating in 3nm

R. Shivnaraine[1], *C. Boecker*[1], *E. Groen*[1], *S. Li*[1], *P. Lu*[1], *S. Vamvakos*[1], *R. Vu*[1], *C. Hanke*[1], *S. Tangirala*[1], *W. Liu*[1], *M. Salik*[2], *K. Bartholomew*[2], *S. Reddy*[2], *A. Tessitore*[2], *A. Shallal*[2], *K. Nallaparaju*[2], *J. Liang*[2], *M. Chen*[2], *S. Desai*[1]

[1]Microsoft, Sunnyvale, CA; [2]Microsoft, Raleigh, NC

2:45 PM

8.4 A 112Gb/s/wire Single-Ended Simultaneous Bi-Directional Transceiver with Dynamic Equalizer for Die-to-Die Interface in 28nm CMOS

Z. Huang[*1], *Z. Wang*[*1], *B. Ye*[2], *T. Ye*[1], *D. Yu*[1], *W. Wang*[1,3], *W. Gai*[1,3]

[1]Peking University, Beijing, China
[2]East China Normal University, Shanghai, China
[3]Beijing Advanced Innovation Center for Integrated Circuits, Beijing, China
*Equally Credited Authors (ECAs)

3:00 PM

8.5 A 112Gb/s 0.76pJ/b Reference-less Mixed-Signal PAM-4 CDR in 28nm CMOS

Z. Zhang[*1,2], *Y. Xu*[*1,2], *J. Liu*[1,2], *N. Wu*[1,2], *Z. Zhang*[1,2], *L. Liu*[1,2]

[1]Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China
[2]University of Chinese Academy of Sciences, Beijing, China
*Equally Credited Authors (ECAs)

Break 3:15 PM

3:35 PM

8.6 A 280mW 112Gb/s PAM-4/NRZ Transceiver for Low-Power IOs in 5nm FinFET Technology

U. Singh[1], K. Thasari[1], N. Nidhi[1], A. Iyer[1], S. Surana[1], B. Dayanik[1], Y. Li[1], M. Torabi[1], J. W. Jung[1], A. Grassi[1], M. Fahimnia[1], H. Kimura[2], F. Bahmani[2], H. Chen[2], A. Wang[2], C. Zhao[2], Y. Fang[2], A. Chen[3], A. Momtaz[1], N. Kocaman[1]

[1]Broadcom, Irvine, CA
[2]Broadcom, San Jose, CA
[3]Broadcom, Fort Collins, CO

4:00 PM

8.7 A 112Gb/s PAM-4 SBD Transceiver with Mismatch-Compensated 2×VDD Hybrid and Two-Step Echo Canceller in 28nm CMOS

H. Sun, S. Wei, Y. Su, C. Cao, Y. Zeng, Y. He, Z. Duan, G. Zhang, X. Gui
Xi'an JiaoTong University, Xi'an, China

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8.8 A 0.292pJ/b 56Gb/s/wire Capacitively Driven Simultaneous Bidirectional Transceiver with PVT/Mismatch Tracking for XSR and D2D Interfaces in 28nm CMOS

K. Kim, Y. Lee, D. Na, H-J. Park, J. Song, W-S. Choi
Seoul National University, Seoul, Korea

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8.9 A 72Gb/s/pin Single-Ended Simultaneous Bi-Directional Transceiver with C-Peaking Leakage Cancellation and Dual-Loop Hybrid Impedance Calibration for Chiplet Interfaces

X. Cheng, H. Wu, Z. Li, W. Wu, X. Luo, Y. Zhang, Q. Pan
Southern University of Science and Technology, Shenzhen, China

5:05 PM

8.10 A 180-to-240Gb/s Analog-Intensive PAM-4 Transmitter with 0.70pJ/b Analog Power Efficiency in 65nm CMOS

Z. Lin, H. Jia, W. Deng, S. He, C. Liu, Z. Wang, B. Chi
Tsinghua University, Beijing, China

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8.11 A 1.59pJ/b 112Gb/s PAM-4 and 1.06pJ/b 168Gb/s PAM-8 Resistor-Less 7-Bit SST DAC-Based Transmitter with 8-Tap FFE in 28nm CMOS

Y-H. Tsai, M-H. Chuang, S-I. Liu
National Taiwan University, Taipei, Taiwan

Conclusion 5:35 PM

Wireless Power

Session Chair: Chen-Yen Ho, *MediaTek, Hsinchu, Taiwan*
Session Co-Chair: Jianping Guo, *Sun Yat-sen University, Guangzhou, China*

3:35 PM

9.1 A Single-Power-Link 13.56MHz Wireless Power and Data Transfer System with Synchronized Phase-Shifted Time-Multiplexing Dual Uplinks for Implantable Voltammetry

Z. Li[1], J. Tang[1], N. Singh[2], J. Jiang[1], L. Zhao[1], W. Zhu[1], X. Sun[1], L. Dong[2], C. Huang[1]

[1]Iowa State University, Ames, IA
[2]University of Georgia, Athens, GA

4:00 PM

9.2 A 91%-Efficiency Single-Stage Bipolar Quad-Output Regulating Rectifier with Event-Driven Output Power Enhancement via Coil-Reused DC-DC for Wireless Power Transfer

T. Lu[1], B. Zhao[2], S. Du[1]

[1]Delft University of Technology, Delft, The Netherlands
[2]Zhejiang University, Hangzhou, China

4:25 PM

9.3 An Output-Domain-Independent Single-Transmitter-Dual-Receiver Wireless Power Transfer System with Detuned-Tank and Time-Multiplexing Control for Adaptive Power Distribution

Y. Chen, Y. Lin, D. Chen, J. Guo

Sun Yat-Sen University, Guangzhou, China

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9.4 A Multi-Coil Scalable Energy-Shared Wireless Power Receiver Network for Distributed Time-Division-Multiplexing Somatosensory Cortex Stimulation

K. Cui, Y. Lu

Tsinghua University, Beijing, China

Conclusion 5:15 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 16th, and Tuesday February 17th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2026, as noted by the symbol **DS1**

2.2 A Quad-Chiplet AI SoC with Full-Chip Scalable Mesh Over 16Gb/s UCIe-Advanced Die-to-Die Interface for Large-Scale AI Inferencing

2.3 A 71.3mJ/Frame End-to-End Driving Processor with Flexible Heterogeneous Core Orchestration via Sparsity Reasoning

3.1 A Multimodal Biosensing System-on-Chip with Integrated Wireless Transceiver and Power Management for Stress Monitoring

3.2 A Near-Field RF Reflection Transceiver ASIC for Continuous Unobtrusive Blood Pressure Monitoring

3.3 A Battery-Powered Hybrid Resonant Pulse-Train Generator with Adaptive Frequency Tracking and Residual Energy Recycling for Ultrasonic Implants

3.4 An Ultrasound-Powering TX with Standing-Wave Peak Tracking Employing Adiabatic Power Sensing Achieving 82% Power-Tracking Accuracy and <90ms Settling Time for Brain Implants

3.5 A Simultaneous Wireless Power and Full-Duplex Data Transfer System Over a Single Inductive Link Achieving 17/3.4Mb/s and 61.1% Efficiency for Miniature Biomedical Implants

5.3 SPARTA: A Scalable, Programmable and Active mm-Wave Dual-Surface Reflect/Transmit Array with Integrated Gain and Phase Control Allowing Bidirectional Signal Routing Capability for Robust and Reconfigurable mm-Wave Networks at 60GHz

7.1 54×42 LiDAR 3D-Stacked System-On-Chip with On-Chip Point Cloud Processing and Hybrid On-Chip/Package-Embedded 25V Boost Generation

7.4 A 480×320 CMOS LiDAR Sensor with Tapering 1-Step Histogramming TDCs and Sub-Pixel Echo Resolvers

Demonstration Session 1

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 16th, and Tuesday February 17th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2026, as noted by the symbol **DS1**

10.1 A 3nm, 400TOPS, 1080k DMIPS SoC with Chiplet Support for ASIL D Automotive Cross-Domain Applications

10.6 A Hybrid-Bonded 12.1TOPS/mm² 56-Core DNN Processor with 2.5Tb/s/mm² 3D Network on Chip

13.1 HYDAR: A 390K QPS, 1574K QPS/W Hybrid Analog/Digital Compute-in-RRAM Accelerator for Efficient Recommendation System

13.2 AI-Enabled End-to-End Design in RFICs with Controllable Architectural Style from 'Classical' to 'Non-Intuitive' for mm-Wave/sub-THz LNAs

14.1 THz-TSI: A 0.33pJ/b 264Gb/s Through-Silicon Interconnect Module for 3D Integration Utilizing Terahertz Coupling

14.4 A 40Gb/s 8mW-OMA 1-to-N VCSEL Driver for Parallel and Wireless Optical Links Using 150nm GaN HEMT

16.5 A Single-Inductor Multi-Channel Thermoelectric Energy Harvesting Interface Realizing Uneven Temperature MPPT with 39.6% Efficiency Enhancement and 62mV Tapped-Inductor-Oscillator-Based Start-Up

16.7 A 90.7%-Efficiency Piezoelectric Resonator-Based Sigma Converter with 6-Phase 2-DoF On-Chip Regulation and Zero-Standby Sigma Mode for Transient and Output Power Enhancement

16.10 Fully Integrated mm-Scale 5G RF MIMO Harvester with -40dBm Sensitivity and Spatial MPPT via Hybrid Transformer-Based Combining/Shifting

17.2 The STM32N6 Microcontroller: Enabling Intelligent Edge AI for IoT and Beyond

17.3 ARIES and REGULUS: A Unified and Scalable Hardware-Software Co-Designed NPU SoC Family for On-Device and On-Premises Multimodal Inference

18.3 SMoLPU: 122.1μJ/Token Sparse MoE-Based Speculative Decoding Language Processing Unit with Adaptive-Offload NPU-CIM Core

18.4 SpikeRAM: A 48.1pW/Synapse/Bit Event-Driven Spiking Compute-Near/In-Memory Processor with Neuromorphic Sensor Enabling Life-Long On-Chip Learning

19.8 A Fully Integrated Bidirectional 5-Level Isolated DC-DC Converter with 42.5% Efficiency and 170mW/mm^2 Transformer Power Density

20.8 A 16-to-256QAM G-Band Subharmonic Phase-Modulating Transmitter for Beyond-5G Communications

20.9 A Compact 26/38GHz-Reconfigurable Dual-Band Low-Noise Amplifier Using Transformer-Based Pole-Zero-Inversion Image-Rejection Technique Achieving >39/41dB IRR for 5G Multi-Band Applications

20.10 A 214-to-242GHz Miniaturized Co-Packaged PA-Antenna Array with 29dBm Lens-less EIRP in a 0.13μm SiGe Process

21.7 A Battery-Free Wireless Electrochemical-Interface SoC Featuring 143dB Dynamic Range for Multimodal Wearables

23.2 A 2-Channel 800Gb/s Transceiver for Coherent-Lite Applications with <300ns Latency in 5nm FinFET

23.3 A 2×500Gb/s Monolithic Silicon-Photonic DWDM PAM-4 Transceiver in 45nm CMOS SOI

23.4 A 6.4Tb/s 4.2pJ/b Co-Packaged Optics ASIC with Direct-Drive Integrated TIA and Retimed Segmented Mach-Zehnder Modulator Driver in 7nm FinFET

SESSION 10

Digital Processing and Circuit Techniques

Session Chair: Visvesh Sathe, *Georgia Institute of Technology, Atlanta, GA*
Session Co-Chair: Ping-Hsuan Hsieh, *National Tsing Hua University, Hsinchu, Taiwan*

8:00 AM

10.1 A 3nm, 400TOPS, 1080k DMIPS SoC with Chiplet Support for ASIL D Automotive Cross-Domain Applications

DS1

S. Machida[1], K. Fukuoka[1], T. Onda[1], N. Yada[1], H. Nakano[1], S. Yamanaka[1], H. V. Cao[2], Y. Hara[1], T. Irita[1], K. Wakahara[1], C. Cordoba[3], T. Kamei[1], Y. Shimazaki[1]

[1]Renesas Electronics, Tokyo, Japan
[2]Renesas Design Vietnam, Ho Chi Minh, Vietnam
[3]Renesas Electronics Europe, Paris, France

8:25 AM

10.2 A Dynamic Performance Augmentation in a 3nm-Plus Mobile CPU

C-Y. Lu[1], B-J. Huang[1], S-Y. Hsueh[1], T-H. Tran[1], E-W. Fang[1], C-Y. Yeh[1], Q. Sun[2], T. Chen[2], H. Chen[2], H. Chang[1], C-J. Tsai[1], Y-C. Zhuang[1], B. Chen[1], E. Wang[1], H. Mair[2], S-A. Hwang[1]

[1]MediaTek, Hsinchu, Taiwan
[2]MediaTek, Austin, TX

8:50 AM

10.3 A 2nm Clock-Edge Architecture for Processor Clock-Power Reduction

Y. Peng[1], D. Yingling[1], B. Hajri[2], R. Vachon[1], F. Gebreyohannes[2], V. Li[3], G. Chhetri[4], K. Bowman[1]

[1]Qualcomm, Raleigh, NC
[2]Qualcomm, Cork, Ireland
[3]Qualcomm, San Diego, CA
[4]Qualcomm, Bangalore, India

9:15 AM

10.4 A 0.008mm² 16-to-1600MHz All-Digital Fractional Divider Using AUX-DLL for Background LMS-Based DTC Calibration

A. Elkholy, Y. Ismail, Z. Huang, A. Garg, A. Nazemi, J. Cao, A. Momtaz

Broadcom, Irvine, CA

9:30 AM

10.5 Proactive Power Management-Based Supply Regulation with Online Learning for Variation-Tolerant Workload-Aware Droop Mitigation in 28nm CMOS

X. Chen[1], A. Liss[1], W. Covington[1], Q. Cao[1], Y. Li[1], K. Wei[2], R. Magod[3], M. Khellah[4], X. Zhang[5], J. Gu[1]

[1]Northwestern University, Evanston, IL
[2]Texas Instruments, Dallas, TX
[3]Indian Institute of Technology Madras, Chennai, India
[4]Intel, Hillsboro, OR
[5]IBM T. J. Watson Research Center, Yorktown Heights, NY

Break 9:45 AM

10:05 AM

10.6 A Hybrid-Bonded 12.1TOPS/mm² 56-Core DNN Processor with DS1 2.5Tb/s/mm² 3D Network on Chip

P. C. Knag[1], G. K. Chen[1], S. Xie[2], S. Yada[1], W. Wu[1], Y-S. Lin[1], A. Kashirin[1], X. Meng[2], R. Criss[1], A. S. Leon[3], C. Tokunaga[1], R. K. Krishnamurthy[1], J. W. Tschanz[1]

[1]Intel, Hillsboro, OR
[2]Intel, Austin, TX
[3]Intel, Santa Clara, CA

10:30 AM

10.7 A 28nm Mode-Reconfigurable CAM-CIM Hybrid Complete 3-SAT Solver Supporting Conflict-Driven Clause Learning with 100% Solvability

Z. Wu, X. Tang, L. Lin, Y. Yang, H. Luo, B. Xu, Y. Liang, X. Bo, Y. Wang

Peking University, Beijing, China

10:55 AM

10.8 COBI: A Degree-of-56 Column-Bipartite Densely Connected Digital Ising Chip with 8b Spin Coefficients

Y. Wu[1], J. Bae[1], S. Shin[2], B. Kim[2]

[1]University of California, Santa Barbara, CA
[2]Korea Advanced Institute of Science and Technology, Daejeon, Korea

11:20 AM

10.9 SharpSAT: A Heuristic-Learning-Based SAT Accelerator Achieving 0.8µs/16.1µs Solution Time in SAT/UNSAT Cases

Y. Huang, H. Kong, I. Y. Chou, B. Wang, X. Kong, J. Zhu, L. Li, X. Li, H. Wang, A. Zhang, L. Liu

Tsinghua University, Beijing, China

11:45 AM

10.10 PCIM-SAT: A 55nm Probabilistic K-SAT Solver with p-Bit-Based Parallel-Variable Update on a Mixed-Signal Compute-in-Memory Architecture

T. Bhattacharya, G. H. Hutchinson, D. Kwon, D. Strukov

University of California, Santa Barbara, CA

Conclusion 12:00 PM

SESSION 11

Pipeline and Ultra-High-Speed Data Converters

Session Chair: Shahrzad Naraghi, *ANAFLASH, Sunnyvale, CA*
Session Co-Chair: Chin-Yu Lin, *Mediatek, Hsinchu, Taiwan*

8:00 AM

11.1 A 14b 400MS/s TDC-Assisted Pipelined-SAR ADC with Rail-to-Rail Input VTC and Background Time-Domain Error Calibration

J. Wang[1], B. Li[1], H. Luo[1], M. Zhan[2], X. He[2], D. Shen[1], L. Jie[2], X. Tang[1]
[1]Peking University, Beijing, China
[2]Tsinghua University, Beijing, China

8:25 AM

11.2 A 28nm CMOS SAR-Based Continuous-Time Pipeline ADC with 103dB SFDR and 270MHz Bandwidth Using NCF and DAC Error Calibration

Q. Liu[1], R. Rutten[1], M. Bolatkale[1], A. Aralioglu[1], G. Hardeman[1], E. Siby[1], P. van Mourik[1], V. Ilamurugan[2], S. Bajoria[1], L. Breems[1]
[1]NXP Semiconductors, Eindhoven, The Netherlands
[2]NXP Semiconductors, Delft, The Netherlands

8:50 AM

11.3 A 500MS/s 12b Pipe-SAR ADC Using a Triple-Cascode FIA with Virtual Supply Extension

M. Rocco[1], G. Zanoletti*[1], A. Ceroni*[1], G. Tombolan[1], G. Bè[1,2], L. Ricci[1], S. Levantino[1], A. L. Lacaita[1], L. Bertulessi[1], C. Samori[1], A. G. Bonfanti[1]*
[1]Politecnico di Milano, Milan, Italy
[2]*now with Infineon Technologies, Villach, Austria
*Equally Credited Authors (ECAs)

9:15 AM

11.4 A 13b 500MS/s 94dB-SFDR Resistive-Input Pipelined-SAR ADC with Linear and Efficient Current-Buffer-Based Integrating Sampler

X. He, M. Gu, Y. Tao, S. Huang, Z. Zhang, Y. Zhong, N. Sun, L. Jie
Tsinghua University, Beijing, China

Break 9:40 AM

10:05 AM

11.5 A Compact 7b 175GS/s Linearized Time-Interleaved Slope ADC with Switched Input Buffers

E. Martens, A. Parisi, A. Kankuppe, A. Cooman, H. Li, S. Van Winckel, P. Renukaswamy, L. Moura Santana, J. Lagos Benites, N. Markulic, J. Craninckx

imec, Leuven, Belgium

10:30 AM

11.6 An 8b 20GS/s Time-Interleaved ADC with 2.6mW 1GS/s Hybrid-Voltage/Time-Domain Sub-ADC in 12nm FinFET

D. Miyazaki, Y. Yagishita, M. Takasaki, S. Nagata, T. Nogamida, Y. Abe, K. Tomita, K. Hasebe, T. Kikkawa, S. Yoshizawa, A. Suzuki, S. Kato, T. Naito, K. Bunsen, T. Matsumoto, Y. Katayama

Sony Semiconductor Solutions, Atsugi, Japan

10:55 AM

11.7 A 12b 12GS/s Two-Way Interleaved Pipeline ADC with Integrated Broadband RF VGA in 5nm

H. Zhu[1], L. Singer[1], R. Kapusta[1], D. Kelly[1], T. Pan[1], M. Hensley[2], S. Bardsley[3], C. Dillon[3], D. Rey-Losada[4], K. M. Sheikh[5], C-K. Hsu[1], Z. Li[6], J. Brunsilius[4], E. Alvarez-Fontecilla[4], R. Bishop[1], P. Wilkins[1], H. L'Bahy[1], A. Cantoni[1], N. Zhang[1], K. M. S. Oo[1], C. Asci[1]

[1]Analog Devices, Wilmington, MA
[2]Analog Devices, Austin, TX
[3]Analog Devices, Durham, NC
[4]Analog Devices, San Diego, CA
[5]Analog Devices, Ottawa, Canada
[6]Analog Devices, Toronto, Canada

11:20 AM

11.8 A 14b 20GS/s RF-Sampling DAC Achieving 70.4dBc IMD3 up to 8.9GHz

H. Luo, Z. Long*, W. Zhu, H. Lu, Y. Fu, M. Lei, C. Wang, X. Zhu, Y. Diao, H. Zhu, J. Zhong, L. Tian, Y. Yang, X. Geng, K. Ouyang*

Sanechips Technology, Shenzhen, China
*Equally Credited Authors (ECAs)

Conclusion 11:45 AM

Frequency Synthesizers and VCOs

Session Chair: Dmytro Cherniak, *Marvell Technology, Santa Clara, CA*
Session Co-Chair: Ping Lu, *NVIDIA, Seattle, WA*

8:00 AM

12.1 A 74fs-Jitter, –59dBc-Spur Fractional-N DPLL Using a Supply-Resilient Time-Amplifying Dual-Ramp DTC

R. Gurbaxani[1], C. S. Vaucher[1,2], M. Babaie[1]

[1]TU Delft, Delft, The Netherlands
[2]NXP Semiconductors, Eindhoven, The Netherlands

8:25 AM

12.2 A Fractional-N Digital PLL with a Supply-Insensitive DTC Achieving –62dBc Spur and 69fs Jitter Under 10mV$_{pp}$ Sinusoidal DTC Supply Ripple and 6.2mV$_{rms}$ DTC Supply Noise

D. Fagotti, R. Moleri, M. Rossoni, D. Lodi Rizzini, P. Salvi, S. Gallucci, G. R. Trotta, A. L. Lacaita, S. M. Dartizio, S. Levantino

Politecnico di Milano, Milan, Italy

8:50 AM

12.3 A –66dBc-Worst-Fractional-Spur and 58fs-Jitter Fractional-N Digital PLL Using a Supply-Resilient Pseudo-Differential Inverse-Constant-Slope DTC

P. Salvi, M. Rossoni, R. Moleri, D. Lodi Rizzini, D. Fagotti, S. Gallucci, A. L. Lacaita, S. M. Dartizio, S. Levantino

Politecnico di Milano, Milan, Italy

9:15 AM

12.4 A 21.6fs$_{rms}$-Jitter, -260.7dB-FoM Fractional-N PLL Enabled by an Intrinsically Linear Variable-Slope SPD for Quantization Error Cancellation

Y. Liu, Y. Li, K. Wang, X. Yu, R. Ni

Fudan University, Shanghai, China

Break 9:40 AM

10:05 AM

12.5 A 14GHz Chopper-Refolding Sampling PLL Achieving 33.8fs$_{rms}$ and 80.8dBc Reference Spur with a kT/C-Noise-Cancellation SPD

Y. Liu, J. Zhang, X. Liu, Y. Wang

Tsinghua University, Beijing, China

10:30 AM

12.6 A 0.65-to-1V-V_{DD} 10.5-to-11.85GHz Fractional-N Sampling PLL Achieving 71.47fs Integrated Jitter and <-60dBc Near-Integer Fractional Spur in 40nm CMOS

Y. Li[1,2], J. Chen[1,2], X. Shen[1], J. Yang[3], J. Liu[1,2], N. Wu[1,2], Z. Zhang[1,2], L. Liu[1,2]

[1]Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China

[2]University of Chinese Academy of Sciences, Beijing, China

[3]Westlake University, Hangzhou, China

10:55 AM

12.7 A 7.15-to-7.95GHz Magnetically Enhanced Feedforward Waveform-Shaping CMOS Oscillator with Implicit Common-Mode Noise Cancellation Achieving -146.72dBc/Hz PN@1MHz and 190.6dBc/Hz FoM

R. Ma, W. Deng, H. Jia, J. Lan, Z. Wang, B. Chi

Tsinghua University, Beijing, China

11:20 AM

12.8 A 5.7mW@0.55V-to-50mW@0.9V Deeply Power-Scalable Reconfigurable Series-Resonance/Class-F VCO with Mutual-Inductance Self-Cancellation and Hybrid 8-Shaped Coupling Techniques

J. Lan, W. Deng, H. Jia, S. Zhang, Z. Wang, B. Chi

Tsinghua University, Beijing, China

11:35 AM

12.9 A 10.2-to-16.2GHz Dual-Mode-Transformer-Based Wideband Series-Resonance VCO Achieving >201.1dBc/Hz FoM$_T$ at a 10MHz Offset

Y. Li, Y. Liu, K. Wang, D. Pu, X. Yu, R. Ni

Fudan University, Shanghai, China

Conclusion 11:50 AM

Circuits for AI and AI for Circuits

Session Chair: Minyoung Song, *Daegu Gyeongbuk Institute of Science and Technology, Daegu, Korea*
Session Co-Chair: Chris Rudell, *University of Washington, Seattle, WA*

8:00 AM

13.1 HYDAR: A 390K QPS, 1574K QPS/W Hybrid Analog/Digital Compute-in-RRAM Accelerator for Efficient Recommendation System

DS1

J. Li[1], P. Yao[1], X. Li[1], Z. Hao[1], D. Wu[1], Z. Li[1], H. Xianyu[2], L. Li[3], S. You[4], T. Chiu[5], M. Sheng[6], W. Yang[7], Q. Zhang[1], J. Tang[1], H. Qian[1], B. Gao[1], H. Wu[1]

[1]Tsinghua University, Beijing, China
[2]Beijing Elemem Technology, Beijing, China
[3]Migu Culture Technology, Beijing, China
[4]China Mobile Research Institute, Beijing, China
[5]Xiamen Industrial Technology Research Institute, Fujian, China
[6]Bytedance China, Beijing, China
[7]Huawei Technologies, Shenzhen, China

8:25 AM

13.2 AI-Enabled End-to-End Design in RFICs with Controllable Architectural Style from 'Classical' to 'Non-Intuitive' for mm-Wave/sub-THz LNAs

DS1

J. Zhou[*1], E. A. Karahan*[*2], J. Park[1], S. Ghozzy[1], K. Sengupta[1]*

[1]Princeton University, Princeton, NJ
[2]now with Marvell, Irvine, CA
*Equally Credited Authors (ECAs)

8:50 AM

13.3 Medusa: A Quantum-Inspired 200-Variable 1016-Clause Analog *k*-SAT Solver

L. D. Wormald, Y-T. Hsu, E. Dikopoulos, W. Tang, B. Datsko, A. Hammoud, Z. Zhang, M. P. Flynn

University of Michigan, Ann Arbor, MI

9:15 AM

13.4 An Inverse-Designed Passively Coupled N-Path Filter with g_m-Boosted Active HBT Switches

V. Chenna, H. Hashemi

University of Southern California, Los Angeles, CA

9:30 AM

13.5 A Nonintuitively Frequency-Staggered Wideband mm-Wave Low-Noise Amplifier

V. Chenna, H. Hashemi

University of Southern California, Los Angeles, CA

Break 9:45 AM

Unusual Interconnects and Other Uses for Light

Session Chair: Uygar Avci, *Intel , Hillsboro, OR*
Session Co-Chair: Guy Torfs, *Ghent University, Ghent, Belgium*

10:05 AM

14.1 THz-TSI: A 0.33pJ/b 264Gb/s Through-Silicon Interconnect Module for 3D Integration Utilizing Terahertz Coupling DS1

C. Jiang, X. Feng, X. Shen, C. Chen, Q. Liu, M. Liu, N. Xu

Fudan University, Shanghai, China

10:30 AM

14.2 An 8λ×38Gb/s/λ 106fJ/b Optical WDM Transmitter in 45nm CMOS SOI

A. Shoobi, K. Omirzakhov, Z. Yu, A. Pirmoradi, F. Aflatouni

University of Pennsylvania, Philadelphia, PA

10:55 AM

14.3 A Single-Chip Laser Diode Driver with Built-In Frequency-Sweep Linearization for FMCW LiDAR

W. Zhu[1], J. Jiang[1], X. Sun[1], Z. Li[1], T. Gu[2], X. Zhang[3], C. Huang[1]

[1]Iowa State University, Ames, IA
[2]University of Delaware, Newark, DE
[3]IBM T. J. Watson Research Center, Yorktown Heights, NY

11:20 AM

14.4 A 40Gb/s 8mW-OMA 1-to-N VCSEL Driver for Parallel and Wireless Optical Links Using 150nm GaN HEMT DS1

S. S. Feng[1], F. Chen[1], R. M. Ma[1,2], H. B. Bao[1], K. Zhong[3], P. T. A. Lau[3], C. P. Yue[1,2]

[1]Hong Kong University of Science and Technology, Hong Kong, China
[2]High5 Semiconductor, Hong Kong, China
[3]Hong Kong Polytechnic University, Hong Kong, China

11:35 AM

14.5 Highly-Integrated Light-Sensing System with RF Harvesting and Transmission in Commercial N-Type IGZO Flexible Technology

M. Privitera[1,2], M. Z. Naveed[1], A. Ballo[1,2], G. Giustolisi[1], A. D. Grasso[1], M. Alioto[2]

[1]University of Catania, Catania, Italy
[2]National University of Singapore, Singapore, Singapore

11:50 AM

14.6 Self-Programmable Twin PUFs via Photovoltaic Energy Harvesting During the Pre-Wafer-Dicing Stage

E. Lee, J. Jung, M. Ashok, A. P. Chandrakasan, R. Han

Massachusetts Institute of Technology, Cambridge, MA

Conclusion 12:05 PM

SESSION 15

DRAM, SRAM, and Non-Volatile Memories

Session Chair: Hidehiro Shiga, *KIOXIA, Yokohama, Japan*
Session Co-Chair: Gunther Lehmann, *Infineon Technologies, Neubiberg, Germany*

8:00 AM

15.1 A 2Tb 4b/Cell 6-Plane 3D-Flash Memory with 37.6Gb/mm² Bit Density and >85MB/s Write Throughput

J. M. Thimmaiah[1], R. Yamashita[2], I-S. Yoon[3], J. Li[3], C. Hsu[3], T. Ariki[2], N. Ookuma[2], Y. Kato[2], K. Hayashi[2], K. Yamauchi[2], I. K V[1], M. Kano[2], S. Bhamidipati[1], S. Bhatia[1], S. Malhotra[1], N. Ojima[2], E. Wu[3], Z. Yang[3], F. W. Tsai[3], M. Bayle[2], N. Minami[2], Y. Fujihara[2], K. Kitamura[2], T. Kitani[2], T. Kodama[4], T. Handa[4], N. Kanagawa[4], Y. Ishizaki[4], S. Fujimura[4], Y. Suzuki[4], M. Sako[4], Y. Higashi[4], Y. Watanabe[4], T. Kouchi[4], A. V[1], C-Y. Chen[3], X. Yang[3], G. Liang[3], J. Wang[3]

[1]Sandisk, Bengaluru, India; [2]Sandisk, Yokohama, Japan
[3]Sandisk, Milpitas, CA; [4]KIOXIA, Yokohama, Japan

8:25 AM

15.2 A 350mV Single-Rail SRAM Using Custom-Logic-Bitcell in 2nm-CMOS-Nanosheet Technology for Mobile and Edge-AI Applications

M. Trivedi[1], S. Sinha[1], R. Halli[1], G. Gurumurthy[1], J. Singh[1], C-Y. Cheng[2], L. Chen[2], J. Lin[2], H. Mair[3]

[1]MediaTek, Bengaluru, India; [2]MediaTek, Hsinchu, Taiwan
[3]MediaTek, Austin, TX

8:50 AM

15.3 An 8nm eMRAM for Auto-G1 with Read-Speed of 125MHz and 19.94Mb/mm² at 0.60V

H. Shin[1], G. Kang[1], Y. Kim[1], D. Kim[1], K. Kim[1], S. Lee[1], H. Lee[1], S. Won[1], M. Kim[1], J. Lee[1], S. Ko[2], J. Shim[2], S. Han[1], K. Suh[1], S. Hwang[1], H. Lee[1], J. Jung[1], S. Baek[1]

[1]Samsung Semiconductor, Gyunggido Kiheung, Korea
[2]Samsung Semiconductor, Gyunggido Hwasung, Korea

9:15 AM

15.4 A 16nm 168Mb Embedded STT-MRAM with 0.0249µm² Bit-Cell, Dual-Port Access, and 51.2Gb/s Read Throughput for Automotive and Edge AI Applications

P-H. Lee[1], C-F. Lee[1], H-J. Lin[1], C-H. Lu[1], Y-A. Chang[1], P. W. Sanjaya[1], C-J. Tsen[1], K-C. Chen[1], M-C. Lin[1], C-J. Hung[1], T-L. Chou[1], C-H. Weng[2], C-Y. Wang[2], J. Wu[2], H. Chuang[2], Y. Wang[1], Y-D. Chih[1], T-Y. J. Chang[1]

[1]TSMC Design Technology, Hsinchu, Taiwan; [2]TSMC, Hsinchu, Taiwan

9:30 AM

15.5 A 3nm 0.167fJ/b 5.27Mb/mm² Configurable TCAM with Macro-Wise Pipelined Search Methods for Automotive Applications

S. Nagata, Y. Sawada, K. Takiguchi, M. Morimoto, S. Tanaka, N. Fujita, T. Miura, D. Nakamura, T. Ito

Renesas Electronics, Tokyo, Japan

Break 9:45 AM

10:05 AM

15.6 A 36GB 3.3TB/s HBM4 DRAM with Per-Channel TSV RDQS Auto Calibration and Fully-Programmable MBIST

S. Joo, J. Kim, Y. Lee, J-Y. Kim, Y. Lee, Y-M. Kim, C. Oh, K-H. Shim, H. Lee, Y-Y. Byun, C. Bae, J. Kim, J-M. Ryu, S-H. Kang, J. Lee, Y-U. Chang, J. Lee, J. Hwang, D. Seo, K-H. Na, Y. G. Song, D. Lim, K-S. Ha, Y-S. Sohn, S-J. Hwang

Samsung Electronics, Hwaseong, Korea

10:30 AM

15.7 A 1cnm 14.4Gb/s/pin 16Gb LPDDR6 SDRAM with Efficiency Mode, LDO-Based WCK Tree, Dynamic Write NT-ODT, Fast CS Control and System Meta Mode

J. You, M. Kim*, D. Kwon, S. Yoon, J. Park, H. Do, J. Park, Y. Jung, S. Lee, K. Kim, H. Jeong, J. Kang, H. Kwon, M. Oh, J. Kim, J. Oh, G-M. Hong, D. Ka, S. Lee, H. Song, M. Kim, D. Yun, S. Kwon, D. Lee, T. Shin, J. Lee, J. Yoon, K. Kang, S. Heo, D. Kim, J. Jang, H. Kim*

SK hynix, Icheon, Korea
*Equally Credited Authors (ECAs)

10:55 AM

15.8 A 16Gb 12.8Gb/s LPDDR6 SDRAM with 12-DQ/Sub-Channel Wide NRZ Signaling and Enhanced Reliability by Per-Row Activation Counting and Meta-Data Scheme

K. Kim, Y. Um, H-J. Song*, J. Jang, S. Lee, H. Seol, H-J. Kwon, J-H. Seol, H. Shin, J. Lee, J. Choi, S-W. Yoon, S. Y. Kim, D. Lee, M. Jang, D. Kwon, S. Lee, J. Kim, J. Kim, I. Jung, T. Song, C. W. Kim, S. H. Baek, J. Choi, Y-H. Seo, W. H. Choi, C. Yoo, S. Hwang*

Samsung Electronics, Hwaseong, Korea
*Equally Credited Authors (ECAs)

11:20 AM

15.9 A 48Gb/s 24Gb GDDR7 DRAM for Mid-Range Inference AI with Symmetric 2CH-Mode Operation, Clock-Path Optimization, and RAS Features

H. Park, S. Lee*, K. Kim, J. Cha, H. Ko, J. Yang, S. Kim, Y. Kim, M. Park, G. Lee, K. Lee, S. Lee, J. Lee, G. Jeon, S. Jeong, Y. Joo, J. Cha, S. Hwang, S. Kim, E. Song, J. Ji, B. Kang, B. Kim, S. Byeon, H. Chi, H. Kim, J. Kim*

SK hynix Semiconductor, Icheon, Korea
*Equally Credited Authors (ECAs)

11:45 AM

15.10 A Vertical-Cell-Transistor(VCT)-Based 4F² DRAM with Cell-on-Peripheral (COP) Architecture Using Wafer-to-Wafer Hybrid Copper Bonding

H. Yoon, Y. Park, T. J. Park, S. L. Kim, S. Jung, D. Kim, K. Kim, Y. Kim, K. Kang, B. Won, S-H. Jung, S. Woo, D. Kim, J. Kim, I. Jung, J. Kim, J-J. Song, I. Nam, Y-H. Seo, S. Yim, J. Park, C. Yoo, S. Hwang

Samsung Electronics, Hwaseong, Korea

Conclusion 12:00 PM

Energy Harvesting, Piezo and Chargers

Session Chair: Sung-Wan Hong, *Sogang University, Seoul, Korea*
Session Co-Chair: Kousuke Miyaji, *Shinshu University, Nagano, Japan*

8:00 AM

16.1 PV Energy-Harvesting Interface Using Reconfigurable Self-Clamp CSCR Converter Achieving 3.83× High-Efficiency VCR Ratio and Open-Voltage-Sense-Free MPPT

Z. Zhong, R. P. Martins, M. Huang
University of Macau, Macau, China

8:25 AM

16.2 A Bias-Flip-Based Piezoelectric Energy Harvesting Interface with a Digital Track-and-Lock MPPT Achieving Sampling-Free Operation and 99.8% MPPT Efficiency

R. Zhang[1], C. Wang[2], Z. Ye[1], K. N. Leung[2], J. Guo[1]
[1]Sun Yat-Sen University, Guangzhou, China
[2]Chinese University of Hong Kong, Hong Kong, China

8:50 AM

16.3 A Fully Integrated Piezoelectric Energy-Harvesting Interface with Single-Stage Bias-Flip and MPPT Achieving 5.63× Maximum Output Power Improving Rate

X. Wu[1], J. Yuan[1], M. Shang[1], B. Wang[1], S. Du[2], L. Cheng[1]
[1]University of Science and Technology of China, Hefei, China
[2]TU Delft, Delft, The Netherlands

9:15 AM

16.4 A One-Stage Bidirectional Rectifier with Pre-Charge-Based MPPT for Triboelectric Energy Harvesting with 93% MPPT Efficiency and 8.86× Power Enhancement

W. Peng, J. Peng, W. van Driel, G. Zhang, S. Du
Delft University of Technology, Delft, The Netherlands

9:30 AM

16.5 DS1 A Single-Inductor Multi-Channel Thermoelectric Energy Harvesting Interface Realizing Uneven Temperature MPPT with 39.6% Efficiency Enhancement and 62mV Tapped-Inductor-Oscillator-Based Start-Up

Y. Yang, S. Du
Delft University of Technology, Delft, The Netherlands

Break 9:45 AM

10:05 AM

16.6 A Parameter-Free Runtime-Energy-Loss Optimizer Achieving 2.15% Error in Energy-Recycling Duty-Cycled Systems

J. Yang, R. P. Martins, M. Huang

University of Macau, Macau, China

10:30 AM

16.7 DS1 A 90.7%-Efficiency Piezoelectric Resonator-Based Sigma Converter with 6-Phase 2-DoF On-Chip Regulation and Zero-Standby Sigma Mode for Transient and Output Power Enhancement

S. Jiang[1], T. Wang[1], P. Mercier[2], S. Du[1]

[1]Delft University of Technology, Delft, The Netherlands
[2]University of California, San Diego, CA

10:55 AM

16.8 A Battery Charger Based On Mesh-Connection 2×CF Continuously-Scalable-Conversion-Ratio Converter Achieving 3.2W/mm³ Power Density

Y. Wang[1], Z. Zhang[1], Y. Zhang[2], R. P. Martins[1], M. Huang[1]

[1]University of Macau, Macau, China
[2]Hong Kong University of Science and Technology, Hong Kong, China

11:20 AM

16.9 A 96.6% Single-Mode Hybrid Dual-Path Buck-Boost Converter with Conduction Loss Reduction through Conversion-Ratio-Based Adaptive 3-Phase Control

M. Kim[1], Y. Lee[1], H. Park[1], H. Kim[1,2], W. Jung[1,2], M. Kim[2], J. Bae[2], H-S. Oh[2], H. Yu[2], H-M. Lee[1]

[1]Korea University, Seoul, Korea
[2]Samsung Electronics, Hwaseong, Korea

11:35 AM

16.10 DS1 Fully Integrated mm-Scale 5G RF MIMO Harvester with -40dBm Sensitivity and Spatial MPPT via Hybrid Transformer-Based Combining/Shifting

A. Ballo[1,2], R. Yang[2], K. Ali[2], M. B. Alioto[2]

[1]University of Catania, Catania, Italy
[2]National University of Singapore, Singapore, Singapore

Conclusion 11:50 PM

Highlighted Chip Releases for AI

Session Chair: Hugh Mair, *MediaTek, Austin, TX*
Session Co-Chair: Sylvain Clerc, *CEA LIST, Grenoble, France*

1:30 PM

17.1 NVIDIA GB10: SoC Built for AI Acceleration

A. Skende[1], G. Rosseel[2], N.Pinckney[3]

[1]Nvidia, Westford, MA
[2]Nvidia, Santa Clara, CA
[3]Nvidia, Austin, TX

1:55 PM

17.2 The STM32N6 Microcontroller: Enabling Intelligent Edge AI for IoT and Beyond

DS1 DS2

G. Desoli[1], J-F. Agaësse[2], N. Chawla[3], E. Hilkens[2], T. Boesch[4], V. Taufour[2], M. Ayodhyawasi[3], P. Ravenhill[2], S. Pal-Singh[3], M. Soulie[2]*

[1]STMicroelectronics, Cornaredo, Italy
[2]STMicroelectronics, Grenoble, France
[3]STMicroelectronics, Greater Noida, India
[4]STMicroelectronics, Geneva, Switzerland

2:20 PM

17.3 ARIES and REGULUS: A Unified and Scalable Hardware-Software Co-Designed NPU SoC Family for On-Device and On-Premises Multimodal Inference

DS1 DS2

D. Shin, H. Yang, S. Jeon, J. Park, S. Han, J. Park, J. Lee, J. Kim, H. Kim, Y. Oh, M. Kim, C. Jung, W. Kim, S. Kim, H. Jeong, G. Kim, K. Lee, G. Song, Y. Min, C. Song, A. Kanybek, Y. Jung, J. Song, S. Cho, H. Na, J. Park, D. Si, B. Lee, B. Park, H. Jeon

Mobilint, Seoul, Korea

2:45 PM

17.4 MAIA: A Reticle-Scale AI Accelerator

S. Xu[1], G. Mandal[1], S. Jahagirdar[1], S. Tripathy[2], P. Parthasarathy[1], S. Srinivasan[1], A. Levin[1]

[1]Microsoft, Mountain View, CA
[2]Microsoft, Bengaluru, India

Break 3:10 PM

Technology and Circuits for Domain-Specific Accelerators

Session Chair: Dongsuk Jeon, *Seoul National University, Seoul, Korea*
Session Co-Chair: Carlos Tokunaga, *Intel, Hillsboro, OR*

3:35 PM

18.1 A 3.19pJ/b Electro-Optical Router with 18ns Setup Frame-Level Routing and 1-to-6 Wavelength-Flexible Link Capacity for Photonic Interposers

Y. Thonnart[1], C. Bernard[2], S. Bernabé[2], M. Assous[2], L. Boutafa[2], B. Charbonnier[2], R. Franiatte[2], C. Fuguet[1], O. Guille[2], V. Josselin[2], S. Malhouitre[2], L. Mendizabal[2], A. Myko[2], D. Saint Patrice[2], R. Vélard[2], J. Charbonnier[2]

[1]CEA-List, Grenoble, France; [2]CEA-Léti, Grenoble, France

4:00 PM

18.2 A 22nm 1.87ms/Frame Streaming Multi-Speaker ASR Accelerator Leveraging Contextual-Aware Redundancy Skipping with 2D-Writable Microscaling Compute-in-Memory and Similarity-Aware TCAM Design

W. Ren, M. Li*, Z. Jin, Y. Ding, R. Xu, X. Ye, Y. Ma, T. Jia, L. Ye*

Peking University, Beijing, China
*Equally Credited Authors (ECAs)

4:25 PM

18.3 SMoLPU: 122.1μJ/Token Sparse MoE-Based Speculative Decoding Language Processing Unit with Adaptive-Offload NPU-CIM Core

DS1

S. Ha[1], J. Lee[1], Y. Moon[1], S. Whang[1], W. Jo[1], G. Park[1], S. Kim[1], S. Um[2], J. Ryu[1], Y. Jo[1], H-J. Yoo[1]

[1]KAIST, Daejeon, Korea
[2]Massachusetts Institute of Technology, Cambridge, MA

4:50 PM

18.4 SpikeRAM: A 48.1pW/Synapse/Bit Event-Driven Spiking Compute-Near/In-Memory Processor with Neuromorphic Sensor Enabling Life-Long On-Chip Learning

DS1

H. Fu[1], Y. Zhou[1], Z. Zhang[1], H. Zheng[1], R. Yang[1], Y. Huang[1], D. Yang[2], Y. Xing[3], T. Demirci[4], N. Qiao[5], B. Cheng[1]

[1]Hong Kong University of Science and Technology, Guangzhou, China
[2]North China Research Institute of Electro-Optics, Beijing, China
[3]SynSense, Chengdu, China; [4]SynSense, Zurich, Switzerland
[5]SynSense, Ningbo, China

5:15 PM

18.5 A 28nm 47.3TFLOPs/W 894mJ/Inference Visual Autoregressive Accelerator with Differential-Amplifier Speculation and Chain-Reaction-Like Parallel Generation.

Z. Yue, X. Xiang*, J. Fu, S. Wei, Y. Wang, Y. Hu, S. Yin*

Tsinghua University, Beijing, China
*Equally Credited Authors (ECAs)

Conclusion 5:30 PM

SESSION 19

High-Voltage, Isolated and Display Power

Session Chair: Xugang Ke, *Zhejiang University, Zhejiang, China*
Session Co-Chair: Yuan Gao, *Southern University of Science and Technology, Shenzhen, China*

1:30 PM

19.1 Piggybacked SC-on-CSCR: A Modular On-Chip Switched-Capacitor Converter for 12-to-60V Input 1.8-to-5V Output Achieving 5.67mW/mm² Power Density and 71.5% Peak Efficiency

Y. Yang[1], X. Zhang[2], S. Du[1]

[1]Delft University of Technology, Delft, The Netherlands
[2]IBM T. J. Watson Research Center, Yorktown Heights, NY

1:55 PM

19.2 A Three-Mode Single-Inductor Four-Quadrant Converter Achieving 94.6% Peak Efficiency with Seamless Zero-Crossing

P. Cao[1,2], J. Xu[2], Z. Hong[2]

[1]Nanjing University, Suzhou, China
[2]Fudan University, Shanghai, China

2:20 PM

19.3 A 94.8%-Peak-Efficiency Double Step-Up SIBO Converter Achieving 88% Output Ripple Reduction for AMOLED Display

H-J. Choi, J-M. Cho, S-Y. Nam, S-W. Hong

Sogang University, Seoul, Korea

2:45 PM

19.4 A Digital-Feedback Active-Gate-Driver IC for 600A 1200V SiC MOSFETs Supporting High- and Low-Side Drive with Simultaneous dV_{ds}/dt Control and V_{ds} Surge Suppression Enabled by Miller Capacitance Calibration

S. Kawai, K. Horii, K. Miyazaki, Y. Bushimata, S. Takaya, H. Ishihara

Toshiba, Kawasaki, Japan

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19.5 A Binary-Weighted Switched-Capacitor Gate Driver IC for Overcoming Trade-offs Between Driving Loss and Delay Time with Gate-Current Feedback Achieving 85% Driving Loss Reduction

K. Horii, K. Miyazaki, S. Kawai, H. Ishihara

Toshiba, Kawasaki, Japan

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19.6 A 68%-Peak-Efficiency Single-Transformer Multi-Output Isolated DC-DC Converter with a Regulated Negative Rail

Q. Huang[*1], *D. Pan*[*1], *W. Xu*[2], *Y. Zhang*[1], *L. Cheng*[1,2]

[1]University of Science and Technology of China, Hefei, China
[2]Hefei CLT Microelectronics, Hefei, China
*Equally Credited Authors (ECAs)

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19.7 A Hybrid Bipolar-Output Isolated Converter with +15V/–5V Outputs for SiC Gate Drivers

J-M. Cho, J-H. Kim, Y-C. Lee, S-W. Hong

Sogang University, Seoul, Korea

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19.8 DS1 A Fully Integrated Bidirectional 5-Level Isolated DC-DC Converter with 42.5% Efficiency and 170mW/mm² Transformer Power Density

K. Datta, Y. Wu, C. Sullivan, J. Stauth

Dartmouth College, Hanover, NH

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19.9 A 2.15W 120V/230Vac to 5-to-12Vdc Offline Power Converter with Full-Duty-Cycle Input-Series Dual-Branch Converter Achieving 1088mW/cm³ and 87.2% Peak Efficiency

G. Liu[1,2], *J. Jiang*[2], *S. Du*[3], *X. Liu*[1]

[1]Chinese University of Hong Kong, Shenzhen, China
[2]Southern University of Science and Technology, Shenzhen, China
[3]TU Delft, Delft, The Netherlands

Conclusion 5:15 PM

SESSION 20

RF Transceiver Subsystems from cm-Wave to THz

Session Chair: Sudipto Chakraborty, *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Session Co-Chair: Mikko Varonen, *VTT Technical Research Centre of Finland, Espoo, Finland*

1:30 PM

20.1 An Ultra-Compact Asymmetrically Load-Pulled Series Doherty Power Amplifier in 22nm FDSOI CMOS with 25.3dBm P_{sat} and 29.7% PAE_{6dB} for Ku-Band 6G FR3

J. Xu[1], T-Y. Huang[1,2], M. Eleraky[1], I. Tolaib[1], H. Wang[1]

[1]ETH Zurich, Zurich, Switzerland
[2]ARGUS SPACE AG, Zurich, Switzerland

1:55 PM

20.2 A High Back-off Efficiency Unequal-Stacked Doherty Power Amplifier Achieving 16.7dBm P_{avg} in a 22nm FDSOI CMOS Technology for 5G FR2 Applications

S. Park, J. Lee, S. Baek, T. Kim, Y. Chen, S. Jeon, S-G. Yang

Samsung Electronics, Seoul, Korea

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20.3 DS2 A mm-Wave Doherty Power Amplifier in a Single-Path Footprint Using Compact Reciprocal Doherty Networks

L. Liu[1], Y. Fang[1], Q. Zhou[2], T. Chi[2], S. Li[1]

[1]University of Texas, Austin, TX
[2]Rice University, Houston, TX

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20.4 DS2 An Ultra-Compact, Inherently Resilient FR3 Source-Follower Power Amplifier with 4:1 VSWR-Resilience and RIMD Immunity for Large-Scale SATCOM and 6G Phased-Arrays

M. Eleraky, J. Zeng, H. Wang

ETH Zurich, Zurich, Switzerland

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20.5 A 24-to-27.5GHz Self-Adaptive Load-Modulated Balanced Amplifier for Integrated Communication, Sensing, and Power Transfer Scenarios

L. Yu[1], P. Chen*[1], Y. Yu[1], G. Zhang[1], X. Lu[1], X. Zhang[2], J. Chen[1], X. Zhu[1], C. Yu[1], W. Hong[1]*

[1]Southeast University, Nanjing, China
[2]China Academy of Information and Communications Technology, Beijing, China
*Equally Credited Authors (ECAs)

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20.6 A 330-to-344GHz GaN Power Amplifier with Maximum-Available-Gain-Boosting Technique and Compact Tandem Coupler Achieving 86mW Output Power at 340GHz

W. Wang[1,2], W. Chen*[3], K. Xie*[4], C. Luo[2], Y. Zhang[2], D. Shang[2], Z. Jiang[2], G. Yu[2], Y. Chen[2], K. Wang[4]*

[1]National Key Laboratory of Solid-State Microwave Devices and Circuits, Nanjing, China
[2]Nanjing Electronic Device Institute, Nanjing, China
[3]Tsinghua University, Beijing, China; [4]Tianjin University, Tianjin, China
*Equally Credited Authors (ECAs)

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20.7 An Ultra-Compact D-Band Transceiver Front-End Based on a Common-Gate Bidirectional Amplifier Achieving 11.2dBm TX P_{sat} and 8.2dB RX Average NF for an Area-Constrained 2D Beamformer AiP

S. M. A. Uddin[1,2], W. Lee[1]

[1]Pennsylvania State University, University Park, PA
[2]Texas Instruments, Dallas, TX

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20.8 DS1 A 16-to-256QAM G-Band Subharmonic Phase-Modulating Transmitter for Beyond-5G Communications

J. Zhou[1], J. Du[1], C-J. Tien[1], J-W. Chen[1], R-C. Soong[1], F. C. Beltran[1], L. Cuskelly[1], C. Chen[1], M. Zhu[1], A. Tang[1,2], S-W. Tam[3], M-C. F. Chang[1]

[1]University of California, Los Angeles, CA
[2]California Institute of Technology, Los Angeles, CA
[3]NXP Semiconductors, San Jose, CA

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20.9 DS1 A Compact 26/38GHz-Reconfigurable Dual-Band Low-Noise Amplifier Using Transformer-Based Pole-Zero-Inversion Image-Rejection Technique Achieving >39/41dB IRR for 5G Multi-Band Applications

J. Luo, J. Wen, Y. Wu, X. Wang, L. Sun

Hangzhou Dianzi University, Hangzhou, China

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20.10 DS1 A 214-to-242GHz Miniaturized Co-Packaged PA-Antenna Array with 29dBm Lens-less EIRP in a 0.13μm SiGe Process

Q. Meng, Z. Wang, P. Zhou, D. Tang, S. Tang, J. Xiao, R. Zhou, J. Li, Z. Chen, J. Chen, H. Gao, W. Hong, Southeast University, Nanjing, China

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20.11 A 215GHz 8×8 Radiator-Oscillator Array with Robust Coupling Achieving 25.5dBm EIRP and 12.9% FTR

A. Elmenshawi[1], S. Muralidharan[2], M. M. Hella[1]

[1]Rensselaer Polytechnic Institute, Troy, NY
[2]Oso Semiconductor, Berkeley, CA

Conclusion 5:35 PM

SESSION 21

Sensor Interfaces

Session Chair: Drew Hall, *University of California at San Diego, La Jolla, CA*
Session Co-Chair: Edoardo Bonizzoni, *University of Pavia, Pavia, Italy*

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21.1 Sub-1mV-Accuracy, 24-CH Synchronous Battery Monitoring IC with Bipolar-Sampling ADCs and Calibration Engines

J. Han[1,2], S. Woo[2], K-S. Oh[2], D. Kim[2], Y. Ko[2], W-J. Choi[1,2], S. Han[2], K. Park[2], J. Choi[2], J. Lee[2], J-Y. Jeon[2], Y-S. Son[2], S-G. Lee[1], K. Kwon[1]

[1]Korea Advanced Institute of Science and Technology, Daejeon, Korea
[2]Autosilicon, Daejeon, Korea

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21.2 DS2 A Fully Integrated GMR Biosensor with On-Chip Coils and Sensors Achieving 605 Resolution FoM for Multiplexed PoC Diagnostics

M. Wu[1], R. Lassalle-Balier[2], P. Aguirre[3], F. Ferrer[3], S. Haji Alizad[4], S. Kummari[1], A. Latham[4], D. A. Hall[1]

[1]University of California, San Diego, CA
[2]Allegro MicroSystems, Chavanod, France
[3]Allegro MicroSystems, Montevideo, Uruguay
[4]Allegro MicroSystems, Manchester, NH

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21.3 A Temperature- and Aging-Compensated TMR Current Sensor with ±0.13% Sensitivity Variation from -40°C to 120°C

T. Qu, N. Wang, K. Zhou, J. Liu, L. Xiang, M. Sun, Z. Hong, X. Zeng, J. Xu

Fudan University, Shanghai, China

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21.4 A Background-Calibrated NPN-Based Temperature Sensor with 0.05°C (3σ) Inaccuracy from -70°C to 125°C

N. G. Toth, K. A. A. Makinwa

TU Delft, Delft, The Netherlands

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21.5 A 0.6V 625um^2 Fully Stacked RC-Based Temperature Sensor Using Low TCR Metal Resistor Achieving 0.017nJ·%^{2}-Accuracy FoM in 2nm Gate-All-Around Process

H. Choi, J. Kim, W. Jung, S. Yoo, J-H. Yang, S. Lee, J. Park, M. Choi, B. Rhew

Samsung Electronics, Yongin, Korea

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21.6 A ±60mA-Inaccuracy Low-Side Average Current Sensor with Operating-Conditions-Insensitive Control Supporting 0.1-to-3A Load Range and Sub-100ns Sample Time for Automotive USB Charge Application

J-J. Kuang[1,2], X. Ming[1], X-C. Gong[1], T-C. Lang[2], X. Geng[2], B. Zhang[1]

[1]University of Electronic Science and Technology of China, Chengdu, China
[2]SouthChip Semiconductor Technology, Chengdu, China

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21.7 A Battery-Free Wireless Electrochemical-Interface SoC Featuring 143dB Dynamic Range for Multimodal Wearables DS1

W. Wang, Y. Shen, T. Cai, Q. Xiao, Y. Luo, B. Zhao

Zhejiang University, Hangzhou, China

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21.8 A CMOS Hybrid Common-Gate Current-Integrating Sampler with >37dB SNDR Across 51GHz BW in a 128GS/s Front-End

J. Dai[1], Y. Zhong[1], Y. Tao[1], A. Zhang[1], M. Zhan[1], H. Zhang[2], L. Jie[1], N. Sun[1]

[1]Tsinghua University, Beijing, China
[2]Magnichip, Nanjing, China

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21.9 A -82.3dB THD+N 60V Fully Integrated Shunt-Resistor-Based In-Line Current Sensor with DLL-Assisted Dynamic Body-Biasing Technique

H. Ma, H. Zhang, Q. Fan

TU Delft, Delft, The Netherlands

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Circuits in Extreme Environments

Session Chair: Giorgio Ferrari, *Politecnico di Milano (IT), Milan, Italy*
Session Co-Chair: Joseph Bardin, *Google & UMass Amherst, Goleta, CA*

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22.1 A Cryo-CMOS Color-Center Quantum Controller with Diamond Waveguide Micro-Chiplet Integration

J. Wang, Y. Han, I. B. Harris, E. Lee, Y. Hu, D. Liu, D. Englund, R. Han

Massachusetts Institute of Technology, Cambridge, MA

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22.2 A 16-Channel Low-Power Cryo-CMOS Flux Control Pulse Generator ASIC in 14nm FinFET Technology

K. Tien[1], D. J. Frank[1], J. F. Bulzacchelli[1], P. Rosno[2], D. Moert[2], J. Timmerwilke[1], A. Noori[1], D. Underwood[1], K. Inoue[1], S. Ray[1], D. Ramirez[2], T. J. Schmerbeck[2], B. Snell[2], J. Ekman[2], R. Black[2], M. Yeck[1], T. Haselhorst[2], E. Erickson[2], K. Demsky[2], C. W. Baks[1], J. Kaus[2], A. Ruffino[3], P. A. Francese[3], A. Davies[2], S. Chakraborty[1], S. Lekuch[1], B. P. Gaucher[1], B. Sadhu[1], S. M. Willenborg[2], D. J. Friedman[1]

[1]IBM T. J. Watson Research Center, Yorktown Heights, NY
[2]IBM Systems, Rochester, MN
[3]IBM Zurich Research Laboratory, Rueschlikon, Switzerland

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22.3 A Multi-Qubit Cryo-CMOS SoC with Polar-Based Electron-Spin and PDM-Based Nuclear-Spin Controllers for Color Centers in Diamond

N. Fakkel, L. Enthoven*, M. A. Elbadry, H. B. van Ommen, M. van Riggelen, J. Yun, T. H. Taminiau, F. Sebastiano**, M. Babaie***

TU Delft, Delft, The Netherlands
*Equally Credited Authors (ECAs)

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22.4 A Radiation-Hardened Self-Healing CMOS Imager with Online Pixel/Logic Annealing and Tile-Adaptive Compression for Space Applications

Q. Cheng[1,2], Z. Yang*[1], H. Li[2], Q. Li[1], Z. Kong[1], G. Niu[1], Y. Liang[1], J. Li[1], J. Yoo[3], M. Hashimoto[2], L. Lin[1]*

[1]Southern University of Science and Technology, Shenzhen, China
[2]Kyoto University, Kyoto, Japan; [3]Seoul National University, Seoul, Korea
*Equally Credited Authors (ECAs)

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22.5 A 500kGy Radiation-Hardened 2.4GHz Wi-Fi Receiver for Innovative Nuclear Power Plant Decommissioning

Y. Narukiyo[1], S. Kato[1], K. Yanaka[1], Y. Takahashi[1], M. Miyahara[2], J. Mayeda[1], A. Shirane[1]

[1]Institute of Science Tokyo, Tokyo, Japan
[2]High Energy Accelerator Research Organization, Ibaraki, Japan

Break 3:15 PM

Next-Generation Optical Transceivers

Session Chair: Ahmed Mostafa, *Marvell, Santa Clara, CA*
Session Co-Chair: Quan Pan, *Southern University of Science and Technology, Shenzhen, China*

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23.1 A 32Gb/s/λ 256Gb/s/Fiber Half-Rate Bandpass-Filtered Clock-Forwarding DWDM Optical Link in a 3D-Stacked 7nm EIC/65nm PIC Technology

S. Song[1], N. Mehta[1], N. Nedovic[1], A. Rekhi[1], G. Kalogerakis[1], L. Xu[1], B. Zimmer[1], S. G. Tell[2], Y. Nishi[1], X. Chen[1], W. Lopes[1], B. G. Lee[3], T. H. Greer III[2], C. T. Gray[2]
[1]Nvidia, Santa Clara, CA; [2]Nvidia, Durham, NC; [3]Nvidia, Ridgefield, CT

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23.2 DS1 A 2-Channel 800Gb/s Transceiver for Coherent-Lite Applications with <300ns Latency in 5nm FinFET

M. Sosio[1], C. Nani[1], E. Monaco[1], N. Ghittori[1], D. Albano[1], A. Di Pasquo[1], A. Bosi[1], T. Lovitt[2], G. Gira[1], F. Martinelli[1], V. Karam[2], D. Khanna[2], M. N. Khiarak[2], S. Cyrusian[3], M. Davoodi[3], M. Garampazzi[1], N. N. Miral[1], F. Giunco[1], I. Fabiano[1], N. Codega[1], C. Asero[1], D. L. Herbas[1], E. Temporiti[1], S. Scouten[2], K. Kota[3], Y. Fu[4], R. Jin[3], J. Mueller[4], M. Leung[3], A. Farhoodfar[4], S. Jantzi[3], K. Chang[4], [1]Marvell, Pavia, Italy; [2]Marvell, Ottawa, Canada; [3]Marvell, Irvine, CA; [4]Marvell, Santa Clara, CA

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23.3 DS1 A 2×500Gb/s Monolithic Silicon-Photonic DWDM PAM-4 Transceiver in 45nm CMOS SOI

Z. Xu, Y. Lin*, J. Jin*, Z. Ye*, D. Xu, A. Xu, C. Sheng, B. Hong, X. Bi*
Huazhong University of Science and Technology, Wuhan, China
*Equally Credited Authors (ECAs)

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23.4 DS1 A 6.4Tb/s 4.2pJ/b Co-Packaged Optics ASIC with Direct-Drive Integrated TIA and Retimed Segmented Mach-Zehnder Modulator Driver in 7nm FinFET

M. Kashmiri, A. Yadav, J. Namkoong, B. Nakhkoob, T. Kao, S. Shen, V. Pandey, K-C. Chen, J. Han, S. Gaddam, S. Kazemkhani, S. Y. Kim, S. Maangat, B. Nguyen, M. Robinson, H. Hedayati, Broadcom, San Jose, CA

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23.5 A 212Gb/s/λ 0.91pJ/b Direct-Drive O-Band Monolithic Coherent Transmitter Based on Carrier-Injection-Mode Mach-Zehnder Modulator

A. R. Chowdhury[1], W. Rahman[1], A. ElShater[2], T. Ali[2], V. Stojanovic[1,3]
[1]University of California, Berkeley, CA; [2]MediaTek, Irvine, CA
[3]Ayar Labs, San Jose, CA

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23.6 A 112Gb/s NRZ Heterodyne Detection 23ns Settled Burst-Mode RX with CD Suppression and Envelope Demodulation for 100G PON

C. Wang, Y. Gu, G. Coudyzer, S. Niu, J. Zhang, X. Yin
imec - Ghent University, Ghent, Belgium

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Displays

Session Chair: Seunghoon Ko, *Kwangwoon University, Seoul, Korea*
Session Co-Chair: Sanshiro Shishido, *Panasonic, Kadoma, Japan*

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24.1 A 28nm CMOS 1-Chip In-Pixel Memory Backplane Circuit with Pixel-Level Sensing and Compensation for 6652-PPI MicroLED AR Glasses

Y. Kwon, S. Kim, Y. Choi, T. Kwon, S. Ryu, S. Na, K. Kim, U. Song, H-W. Lim, J. Lee, J-Y. Lee

Samsung Electronics, Suwon, Korea

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24.2 A 4042-PPI 10b 240Hz Digital-PWM CMOS Backplane for Micro-LED-on-Silicon Displays with a Shared, Unified Memory-in-Pixel Architecture

K. Kim, J-G. Lee, H-S. Kim

KAIST, Daejeon, Korea

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24.3 A 144mW 161Mpixels/s Tensor Display Processor for 3D Virtual Reality

C-Y. Lee, Y-F. Tsai, Y-S. Lin, C-H. Yang

National Taiwan University, Taipei, Taiwan

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24.4 A 512ch 10b Source-Driver IC with Current-Mode Auto-Zeroing Scheme Achieving 1.4mV DVO and 600ns 1-Horizontal Time for Mobile OLED Displays

Y. Park, G-W. Lim, H-S. Kim

KAIST, Daejeon, Korea

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24.5 A 10b Display Driver IC with a Pivoting Translinear-Loop DAC-in-Buffer Enabling 1μs 1-H Scan Time and 1722μm² per Channel

H-J. Kim, Y. Park, K. Kim, S. Shin, H-S. Kim

KAIST, Daejeon, Korea

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24.6 A Touch-Embedded OLED Display-Driver IC with Display Noise Referencing and Display Coupling Noise Prediction Based on Dedicated Neural Networks for Mobile Applications with CoE Display

Y-R. Jo, S. Na, S. Byun, J. Park, G. Ha, J. Ok, T-G. Song, W-N. Lee, J. Lee, H-W. Lim, S. Kim, J-Y. Lee

Samsung Electronics, Hwaseong, Korea

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This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 16th, and Tuesday February 17th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2026, as noted by the symbol **DS2**

2.7 Tiamat: A 98-to-134ms/Step Transformer-Based Diffusion Model Processor Supporting Classifier-Free Guidance for Image Generation

2.10 A 1286fps 0.39mJ/Frame Modeling/Rendering Unified 3D GS Processor with Locality-Optimized Computation and Reconfigurable Architecture

4.3 A 0.6V 9.4μW 1,892μm² Current-Pulse-Injection Crystal Oscillator Featuring Capacitively Biased Amplifier with 242.2dBc/Hz PN FoM @1kHz Offset

4.5 A 1ppm/°C and ±0.066% 3σ Accuracy Bandgap Reference with Temperature-Adaptive PTAT Scaling

6.5 A 26/28/37/39GHz Reconfigurable Fully Connected MIMO Receiver Front-End with On-Chip Diplexer Achieving 52-to-70dB Blocker Rejection

7.8 A 55nm Intelligent Vision SoC Achieving 346TOPS/W System Efficiency via Fully Analog Sensing-to-Inference Pipeline

7.10 A 200MP 0.61μm-Pixel-Pitch CMOS Imager with Sub-1e⁻ Readout Noise Using Interlaced-Shared Transistor Architecture and On-Chip Motion Artifact-Free HDR Synthesis for 8K Video Applications

17.2 The STM32N6 Microcontroller: Enabling Intelligent Edge AI for IoT and Beyond

17.3 ARIES and REGULUS: A Unified and Scalable Hardware-Software Co-Designed NPU SoC Family for On-Device and On-Premises Multimodal Inference

20.3 A mm-Wave Doherty Power Amplifier in a Single-Path Footprint Using Compact Reciprocal Doherty Networks

20.4 An Ultra-Compact, Inherently Resilient FR3 Source-Follower Power Amplifier with 4:1 VSWR-Resilience and RIMD Immunity for Large-Scale SATCOM and 6G Phased-Arrays

21.2 A Fully Integrated GMR Biosensor with On-Chip Coils and Sensors Achieving 605 Resolution FoM for Multiplexed PoC Diagnostics

25.1 HERACLES: 8192-Way SIMD Programmable Scalable Fully-Homomorphic Encryption SoC for Privacy-Preserving Cloud Computing in Intel 3 CMOS

25.3 A 16nm 0.042mm² 0.66uJ/Ops Lightweight MLWE PQC KEM with Cryptanalysis-ASIC Co-optimization

29.1 A 48-Day-Duration Pasting Bioelectronic Device Realizing Closed-Loop Realtime Detection and Precision Treatment for Type-1 Diabetes

29.3 A 256-Channel Event-Driven Readout for Solid-State Nanopore Single-Molecule Sensing with 193pArms Noise in a 1MHz Bandwidth

29.6 A 65nm CMOS Hydrogel-Based Dual Fluorescence Sensor for Bioavailable Phosphorus Detection

30.1 A 28nm 127.54TFLOPS/W MXFP6 and 117.42TFLOPS/W MXFP8 Compute-in-Memory Macro with Adaptive-Preserved-Bit-Width and Serial-Dual-Bit-Sliding Schemes

30.9 A 147TOPS/W, 250TOPS/mm^2, Fully Synthesizable, Digital Compute-in-Memory Accelerator Supporting INT8×INT8 with Zero-Point Quantization in Intel 18A Technology

31.5 SoulMate: A 9.8mW Mobile Intelligence System-on-Chip with Mixed-Rank Architecture for On-Device LLM Personalization

31.9 ALPhA-Vision: A Real-Time Always-On Vision Processor with 787µs Face Detection Latency in <5mW

33.2 An Infinite-Loop CMOS-Compatible Isolator Enabled True VSWR-Resilient Power Amplifier for 6G FR3 in Massive MIMO and Phased-Array Systems

34.1 A 128mW 2×4 Radar-on-Chip with Forward-ΔΣ DPLL-Locked Multi-Injection RTWO in 22nm CMOS Enabling ADC-Free Digitization and PS-Free Beamforming Demonstrated in In-Cabin Vital-Sign Monitoring

34.3 A 234-to-252GHz Dual-Polarized Transceiver Using Antenna-in-Package Technologies for Cross-Polarimetric Sensing

34.4 A 1.6-to-3.8GHz Reconfigurable FMCW Radar SoC with 81.5% Relative-Bandwidth PLL for Real-Time Life Detection in Disaster Response

34.5 A 0.0523mm^2 11.4mW IEEE 802.15.4a/z/ab Compatible Aliasing-Suppressing All-Digital IR-UWB Transmitter Featuring Comb-Notched Maximally Flat Amplitude Spectral Shaping

35.5 Fully Integrated Backscattered WiFi 802.11b Transmitter with Active Harmonics and Image Rejection for 30dB IRR and 36dB HRR at 0.88µW

36.1 ReFIND: A Resolution-Reconfigurable Bio-Signal Classification SoC Enabling >10× Savings in AFE Power per Channel

36.2 A Neural Interface SoC for Smart Glasses with Low-Power Neural Commanding and Efficient LoRA-Enabled On-Chip Learning

36.6 Sparsity-Aware Neural Interface with CIM-Based Predictive Focused Sampling for Hotspot Spike Tracking

36.11 A 0.62µW/sensor 82fps Time-to-Digital Impedance Measurement IC with Unified Excitation/Readout Front-End for Large-Scale Piezo-Resistive Sensor Array

EE2:
Generative AI for Silicon Design: Mastering Complexity, Democratizing Design, and Building Trust

Organizer: **Alfred Yeung,** *AMD, Santa Clara, CA*

Co-Organizers: **Kaushik Vaidyanathan**, *OpenAI, San Francisco, CA*
Julian Tham, *Infineon, San Jose, CA*
Huichu Liu, *Meta Platforms, Sunnyvale, CA*
Cynthia Hsu, *Sandisk, Fremont, CA*
Ping-Hsuan Hsieh, *Nation Tsing Hua University, Tsinchu, Taiwan*
Konstantinos Manetakis, *CSEM, Neuchâtel, Switzerland*
Alberto Valdes-Garcia, *IBM, Yorktown Heights, NY*
Pasqualina Fragneto, *ST Microelectronics, Agrate Brianza, Italy*
Negar Reiskarimian, *MIT, Cambridge, MA*
CM Hung, *Mediatek, Tsinchu, Taiwan*

Moderator: **Siddharth Garg,** *NYU, New York, NY*

Generative AI is rapidly transforming chip design, enabling automation in circuit synthesis, layout, and verification. These advancements promise greater efficiency, but also raise critical questions: What are the fundamental limits of AI-driven automation? Can AI truly match human intuition and creativity? And will it democratize or centralize chip design in the long run? To explore these questions, join us for an engaging evening event featuring a panel of experts at the forefront of AI and VLSI design and an interactive game where we see how far AI in VLSI has come. Through a mix of real-world challenges, live audience interaction, and expert commentary, we'll assess where we are with GenAI in chip design and where we're heading.

Panelists: **Amit Gupta,** *Siemens EDA, Saskatoon, Canada*
Matheus Trevisan Moreira, *Meta, Sunnyvale, CA*
Husni Habal, *Infineon Munich, Munich, Germany*
Azalia Mirhoseini, *Google, Palo Alto, CA*

EE3:
The Augmented Human – Will Chips in Our Brain Enhance Our Cognitive Abilities?

Organizer: **Rikky Muller,** *UC Berkeley, Berkeley, CA*

Co-Organizers: **Hidehiro Shiga,** *KIOXIA, Yokohama, Japan*
Carolina Mora Lopez, *imec, Leuven, Belgium*
SungWon Chung, *Neuralink, Fremont, CA*
Mutsumi Hamaguchi, *Sharp Corporation, Nara, Japan*
Augusto Ximenes, *CogniSea, Seattle, WA*

Moderator: **Azita Emami,** *Caltech, Pasadena, CA*

Can the brain of the future be enhanced with semiconductor technologies? As we deepen our understanding of neural function and continue to miniaturize and integrate advanced electronics, exciting possibilities emerge, such as expanding cognitive capacity through implanted memory, enhancing our vision to perceive unseen wavelengths through visual prostheses, or accelerating thought processes with integrated computational support akin to a co-processor for the brain. While these ideas may lie far beyond current capabilities, this session invites visionary thinkers and cross-disciplinary experts to examine the scientific, technological, and ethical foundations of such a future.

Panelists: **Timothy Denison**, *Oxford University, Oxford, United Kingdom*
Milin Zhang, *Tsinghua University, Beijing, China*
Jan Rabaey, *UC Berkeley, Berkeley, CA*
Dongjin (DJ) Seo, *Neuralink, Austin, TX*

SESSION 25

Hardware Security

Session Chair: Shreyas Sen, *Purdue University, West Lafayette, IN*
Session Co-Chair: Santosh Ghosh, *Nvidia, Hillsboro, OR*

8:00 AM

25.1 HERACLES: 8192-Way SIMD Programmable Scalable Fully-Homomorphic Encryption SoC for Privacy-Preserving Cloud Computing in Intel 3 CMOS

DS2

A. Golder[1], R. Kumar[1], S. Taneja[1], K. Race[2], P. Aseron[1], J. Greensky[1], W. Wang[1], H. Gong[1], L. Kethareswaran[2], V. Suresh[1], A. Vartak[1], A. Challagundla[2], J. Casas[1], P. Lalwaney[1], D. Kim[1], C. N. Gutierrez[1], E. Z. Ramos[1], W. Cho[1], J. M. Rojas Chaves[1], M. Steiner[1], D. Lake[1], N. Yennampelli[3], K. Nivarthi[3], K. Bijinapally[3], B. P. Talamala[3], S. Valluri[3], V. Srirambhatla[3], C. Wilkerson[1], R. Cammarota[1], S. Mathew[1]

[1]Intel, Hillsboro, OR
[2]Intel, Austin, TX
[3]Intel, Hyderabad, India

8:25 AM

25.2 A 28nm 0.48mJ/boot Torus FHE Processor for Arbitrary Computation on Encrypted Data

X. Yu, Y. Sun, Y. Zhao, H. Kuang, S. Wang, Z. Yang, J. Han

Fudan University, Shanghai, China

8:50 AM

25.3 A 16nm 0.042mm² 0.66uJ/Ops Lightweight MLWE PQC KEM with Cryptanalysis-ASIC Co-optimization

DS2

A. Ghosh[*1], M-C. Li*[*1], L. Ding[1], S. Kundu[2], A. Sayeed[1], A. Karmakar[3], H. Naman[1], S. Antal[1], I. Verbauwhede[2], S. Sen[1]*

[1]Purdue University, West Lafayette, IN
[2]KU Leuven ESAT, Leuven, Belgium
[3]Indian Institute of Technology, Kanpur, India
*Equally Credited Authors (ECAs)

9:15 AM

25.4 OmniCrypt: A 435.86M-GOPS/W Bootstrappable Multi-Scheme FHE Accelerator with On-Chip Data Generation for Privacy-Preserving Computation

A. Putra, H. Cho*, S. Yune, C. M. Duong, J. Jeon, J-Y. Kim*

KAIST, Daejeon, Korea
*Equally Credited Authors (ECAs)

9:30 AM

25.5 A 0.05mm² 1.19-to-7.34mW SQIsign-1D Isogeny-Based Post-Quantum Signature Verification Accelerator for IoT

K. S. T. Ramapragada, U. Banerjee

Indian Institute of Science, Bengaluru, India

Break 9:45 AM

10:05 AM

25.6 A 17%/27% Area-/Energy-Overhead Glitch-Transition Secure SHA-3 Engine Fusing Dual-Rail Precharge Logic and Asymmetric Masking

C. Zhao[1,1], H. Shui[1,1], B. Yang[1,1], W. Zhu[1,1], Y. Cao[1,1], Z. Hou[1,1], Y. Liu[1,1], X. Han[1,1], S. Yin[1,1], W. Chen[1,1], H. Wang[1,1], J. Yang[1], M. Zhu[2], A. Zhang[1,1], L. Liu[1,1]

[1]Tsinghua University, Beijing, China
[2]Micro Innovation Integrated Circuit Design, Wuxi, China

10:30 AM

25.7 TinyPAD: A 166μm²/lane Variation-Tolerant Probing-Attack Detector for an 8Gb/s/lane Chip-to-Chip Interface in 16nm FinFET

M. Li[1], R. Wan[1], S. K. Mathew[2], V. De[2], M. Seok[1]

[1]Columbia University, New York, NY
[2]Intel, Hillsboro, OR

10:55 AM

25.8 A Sub-Threshold All-nMOS Reconfigurable PUF with Secure Configuration Selection for Stable 6-Bits/Cell

S. Xu, K. Liu*, L. Chan, H. Tagawa, H. Shinohara, K. Niitsu*

Kyoto University, Kyoto, Japan
*Equally Credited Authors (ECAs)

11:20 AM

25.9 A PVT Variation- and Attack-Tolerant Metastability-Based TRNG Using Binary Search in 2nm

Y. Youn[1], Y. Lim[1,2], J. Lee[1], D. Hong[1], W. Kim[1], Y-S. Kwak[1], K-J. Moon[1], B. Kang[1], S. Yoo[1]

[1]Samsung Electronics, Hwaseong, Korea
[2]now with Yonsei University, Seoul, Korea

11:45 AM

25.10 A 65nm 0.066pJ/bit Floating-Latch-Based True Random Number Generator Resilient to Power-Noise Injection Attacks

K. Cheng[1], Y. Huang[1], Z. Yang[1], L. Wang[1], H. Ren[1], X. Shan[1], P-I. Mak[2], Y. Chen[3], B. Li[1]

[1]Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China
[2]University of Macau, Macau, China
[3]Tsinghua University, Beijing, China

Conclusion 12:00 PM

Compute Power and Supply Modulators

Session Chair: Nicolas Butzen, *Intel, Hillsboro, OR*
Session Co-Chair: Dongsu Kim, *Samsung Electronics, Hwaseong, Korea*

8:00 AM

26.1 Coupled-OSC-Based Converters Achieving 89.5% Peak Efficiency at 61MHz, 1.82W/mm² Power Density at 360MHz, and Inherent Even Phase Interleaving

J. Yang, F. Zhang, R. P. Martins, M. Huang
University of Macau, Macau, China

8:25 AM

26.2 A Compact 4Vin 93.4%-Peak-Efficiency 12A Load and 20mV Undershoot Resonant Sigma Converter with PCB-Embedded Converter-on-Substrate Packaging

Y. Du, S. Ren, Z. Fei, Z. Chen, M. Zhao, C. Li, Y. Ding, W. Li, Z. Tan, W. Qu
Zhejiang University, Hangzhou, China

8:50 AM

26.3 A Multi-Phase Hybrid Converter with Q Samplers Enabling Simultaneous IL Auto-Balance and Arbitrary Phase Count

J. Yang, Z. Tang*, R. P. Martins, M. Huang*
University of Macau, Macau, China
*Equally Credited Authors (ECAs)

9:15 AM

26.4 A 12-to-1V 90.5%-Peak-Efficiency 721A/cm³-Current-Density Quad-Output Converter with One Shared DC Capacitor

Q. Min[1], J. Yuan[1], J. Jin[1], Y. Ji[1], W. Xu[2], L. Cheng[1,2]
[1]University of Science and Technology of China, Hefei, China
[2]Hefei CLT Microelectronics, Hefei, China

9:30 AM

26.5 An Inductor-at-Middle Hybrid Buck Converter with Shared Power-Signal Path for Distributed Vertical Power Delivery

Z. Zhu[1,2], J. Huang[2], Z. Song[1,2], Z. Yu[1,2], S. Han[2], S-W. Sin[2], Y. Lu[1]
[1]Tsinghua University, Beijing, China
[2]University of Macau, Macau, China

Break 9:45 AM

10:05 AM

26.6 A 92.4%-Peak-Efficiency 48V to 0.8-to-1.6V Hybrid Converter with Inductor-Interleaved Fibonacci Switched-Capacitor

H-W. Jeong, C-H. Lee, H-J. Choi, S-W. Hong
Sogang University, Seoul, Korea

10:30 AM

26.7 A 100A 93.4%-Peak-Efficiency LLC Resonant Converter with an Embedded Primary-Current-Extracted Regulator

Z. Liu[1], Y. Ji[1], Z. Luo[1], Y. Ge[1], W. Xu[2], W. Huang[2], L. Cheng[1,2]
[1]University of Science and Technology of China, Hefei, China
[2]Hefei CLT Microelectronics, Hefei, China

10:55 AM

26.8 A 1.2μs 1-to-12V Symbol Power Tracking Supply Modulator with Two-Step Subranging DVS Scheme and Boosted IL Slew Rate for 5G Mobile Devices

C. Chen, M. Shang, Y. Ji, L. Cheng
University of Science and Technology of China, Hefei, China

11:20 AM

26.9 A Compact Dual-Capacitor Relay SPT Supply Modulator with Overshoot-Free Adaptive On-Time Control for 5G FR2 CMOS PA

Z. Yu[1,2], Z. Tong[2], J. Huang[2], J. Yin[2], Y. Lu[1]
[1]Tsinghua University, Beijing, China
[2]University of Macau, Macau, China

Conclusion 11:45 AM

SESSION 27

Frequency Generators, Multipliers, and Modulators

Session Chair: Danilo Manstretta, *University of Pavia, Pavia, Italy*
Session Co-Chair: Teerachot Siriburanon, *University College Dublin, Dublin, Ireland*

8:00 AM

27.1 A 20GHz Frequency Synthesizer with Spur-Shaping Modulator Achieving 46.2fs Jitter and -76.5dBc Worst-Case Fractional Spur

Z. Ye, Y. Sun, L. Hou, Y. Ding, Y. Wen, H. Zhang, X. Geng, Q. Xie, S. Yang, Z. Wang

University of Electronic Science and Technology of China, Chengdu, China

8:25 AM

27.2 A 157fs$_{rms}$-Jitter, –73dBc-Fractional-Spur, Calibration-Free Cascaded SPLL Employing Robust Feedforward Noise Cancellation and MMD-Based Quantization-Error Cancellation with a 60MHz Reference

H. Zhang, Y. He, Y. Zhu, H. Ren, T. Iizuka

University of Tokyo, Tokyo, Japan

8:50 AM

27.3 A 14GHz Ring-Based 3rd-Order Fractional-N PLL with 164fs$_{rms}$ Jitter and a 100MHz Reference

Z. Zhu, Q. Lin, Z. Huang

Hong Kong University of Science and Technology, Guangzhou, China

9:15 AM

27.4 A 0.068mm^2 8.5-to-12.7GHz Complementary Dual-Core VCO with Auto-2nd-Harmonic-Tracking Technique Achieving 202.7dBc/Hz Peak FoM$_T$ and 0.9dB-FoM Variation at a 1MHz Offset in a 39.6% Tuning Range

X. Du[1,2], X. Zhan[1], T. Ou[1], Z. Chen[1], J. Li[1], H. Li[1], Z. Yang[3], Z. Xu[1], P-I. Mak[1], R. P. Martins[1], J. Yin[1]

[1]University of Macau, Macau, China
[2]UM Hetao IC Research Institute, Shenzhen, China
[3]Southwest Jiaotong University, Chengdu, China

9:30 AM

27.5 A 17.9-to-22.4GHz 195.6±1.3dBc/Hz FoM Quad-Core Class-F^{-1} VCO Featuring Improved Synchronization Using a Circular Pentafilar Transformer-Based Tank

Y. Wu[1], Y. Peng[1,2], J. Li[1], F. Yuan[1], J. Li[1], J. Yin[1], R. P. Martins[1], P-I. Mak[1]

[1]University of Macau, Macau, China
[2]UM Hetao IC Research Institute, Shenzhen, China

Break 9:45 AM

10:05 AM

27.6 A 9.7GHz Self-Linearized-VCO-Based FMCW Chirp Generator Achieving 1.56GHz/µs Slope and 0.57µs Duration with 0.094% rms Frequency Error

D. Zhang, Y. Zhang, Z. Liu, Y. Xiong, M. Rossoni, W. Wang, A. A. Fadila, D. Li, M. Tang, D. Xu, C. de Gomez, D. Xu, K. Kunihiro, H. Sakai, K. Okada

Institute of Science Tokyo, Tokyo, Japan

10:30 AM

27.7 A 40.5-to-58.5GHz 36%-Fractional-Chirp-Bandwidth 18GHz-Absolute-Chirp-Bandwidth 2.2GHz/µs-Chirp-Rate 0.02%-Chirp-Error Post-Mixing Bandwidth-Extending Sawtooth-FMCW Frequency Synthesizer Employing a Chirp-Tracking ILFT and a Fractional-Bandwidth Doubler

Y. Liu, Z. Jing*, W. Yang, H. Yang, B. Zhang, H. C. Luong*

HKUST, Hong Kong, China
*Equally Credited Authors (ECAs)

10:55 AM

27.8 A 77GHz 8-bit CMOS Phase Shifter Adopting a Nested-Vector-Based Error Correction with 0.33°/0.07dB RMS-Error for MIMO Radar Applications

G. Park, B-T. Moon, K. Kim, D. Kim, G. Baek, B. Yook, H-C. Park, C-H. Park

Samsung Electronics, Hwaseong, Korea

11:20 AM

27.9 A Dual-Mode DCO-PA with a Twisted 8-Shape Inductor for BLE Achieving 42% TX Efficiency at 1.6dBm and 0.29mW RX Clock

J. Chen[1,2], K. Xu[2], L. Guo[1], T. Siriburanon[1], J. Yin[3], B. M. Al-Hashimi[2], R. B. Staszewski[1]

[1]University College Dublin, Dublin, Ireland
[2]King's College London, London, United Kingdom
[3]University of Macau, Macau, China

11:35 AM

27.10 A 48-to-82.5GHz CMOS Split-Tail Gilbert-Cell Frequency Doubler Achieving 11% PAE at 8.5dBm Output Power

J. Jamal[1], L. Piotto[2], F. Vecchi[3], M. M. Pirbazari[3], A. Mazzanti[1]

[1]University of Pavia, Pavia, Italy
[2]Fondazione Chips-IT, Pavia, Italy
[3]STMicroelectronics, Pavia, Italy

Conclusion 11:50 AM

Innovations from Outside the (ISSCC) Box

Session Chair: Kaushik Sengupta, *Princeton University, Princeton, NJ*
Session Co-Chair: Firooz Aflatouni, *University of Pennsylvania, Philadelphia, PA*

8:00 AM

28.1 Importance of GaN for 5G and Solid-State mm-Wave Circuits of the Future

U. K. Mishra, C. J. Clymore, E. Akso, M. Guidry
University of California, Santa Barbara, CA

8:25 AM

28.2 High-Selectivity, Tunable Filters with Zero Static Power Consumption Formed Using Micromachined Magnetostatic Wave Cavities

S. Yao, X. Du, Y. Ding, S. Wu, C-Y. Chang, M. Allen, R. H. Olsson III
University of Pennsylvania, Philadelphia, PA

8:50 AM

28.3 Body-Interfaced Biosensors

W. Gao
California Institute of Technology, Pasadena, CA

9:15 AM

28.4 The Sensing, Computing, and Devices Opportunities of Computational Behavioral Phenotype: An Autism Spectrum Disorder Case Study

G. Sapiro[1], M. Di Martino[2], G. Dawson[2]
[1]Princeton University, Princeton, NJ
[2]Duke University, Durham, NC

Break 9:40 AM

Biochemical Sensors for Life Sciences and Agriculture

Session Chair: Kaiyuan Yang, *Rice University, Houston, TX*
Session Co-Chair: Albert Wang, *Apple, Cupertino, CA*

10:05 AM

29.1 A 48-Day-Duration Pasting Bioelectronic Device Realizing Closed-Loop Realtime Detection and Precision Treatment for Type-1 Diabetes DS2

X. Wu[*1], *K. Zhao*[*1], *M. Liu*[*1], *S. Ding*[1], *X. Li*[1], *Y. Lu*[1], *R. Wang*[1], *Z. Zhao*[1], *L. Qian*[1], *Y. Yang*[1], *J. Wu*[1], *L. Huang*[1], *C. Shi*[1], *Y. Wei*[1], *Y. Lu*[1], *N. Guan*[1], *H. Ye*[1], *J. Chen*[2], *R. Zhang*[1]

[1]East China Normal University, Shanghai, China
[2]University of Houston, Houston, TX
*Equally Credited Authors (ECAs)

10:30 AM

29.2 A 1400THz/s Ultra-Fast-Scan 14GHz EPR-on-a-Chip Based on Injection-Locked Phase Detection Featuring 120μM Concentration Sensitivity

J-B. David[1], *A. Siligaris*[1], *C. Dehos*[1], *J. L. Gonzalez Jimenez*[1], *J-F. Jacquot*[2], *C. Lombard*[2], *K. Chighine*[2], *V. Maurel*[2], *S. Gambarelli*[2]

[1]CEA-LETI-MINATEC, Grenoble, France; [2]CEA-IRIG, Grenoble, France

10:55 AM

29.3 A 256-Channel Event-Driven Readout for Solid-State Nanopore Single-Molecule Sensing with 193pArms Noise in a 1MHz Bandwidth DS2

S. Crols[1,2], *C. Mora Lopez*[2], *F. Tavernier*[1], *M. Verhelst*[1,2], *N. Van Helleputte*[2]

[1]KU Leuven - MICAS, Leuven, Belgium; [2]imec, Leuven, Belgium

11:20 AM

29.4 Shape-Memory Multi-Size Micro-Cage Array on CMOS with Integrated Electrochemical Sensors for Joint Bio-Sample Manipulation and Sensing

Z. Huang, F. Jiang, H. Liu, A. Wang, Y. Sheng, M. Saif, H. Wang

ETH Zurich, Zurich, Switzerland

11:35 AM

29.5 A Sub-Gram Individual Plant Stress Sensor Tag for Smart Farming

D. Nitto[1], *K. Yanase*[1], *Y. Fujisawa*[1], *J. Shiomi*[1], *Y. Midoh*[1], *T. Wadatsumi*[2], *M. Nagata*[2], *A. Oncu*[3], *C. Sideris*[4], *C. Suriyasak*[5], *Y. Ishibashi*[5], *N. Miura*[1]

[1]University of Osaka, Suita, Japan, [2]Kobe University, Kobe, Japan
[3]Bogazici University, Istanbul, Turkey
[4]University of Southern California, Los Angeles, CA
[5]Kyushu University, Fukuoka, Japan

11:50 AM

29.6 A 65nm CMOS Hydrogel-Based Dual Fluorescence Sensor for Bioavailable Phosphorus Detection DS2

T-Y. Cheng[*], *R. S. Mukkamala*[*], *R. E. Alcalde, M. Panahandeh, A. Agarwal, J. A. Kornfield, D. K. Newman, A. Emami*

California Institute of Technology, Pasadena, CA
*Equally Credited Authors (ECAs)

Conclusion 12:05 PM

SESSION 30

Compute-in-Memory

Session Chair: Vita Pi-Ho Hu, *National Taiwan University, Taipei, Taiwan*
Session Co-Chair: Xueqing Li, *Tsinghua University, Beijing, China*

8:00 AM

30.1 A 28nm 127.54TFLOPS/W MXFP6 and 117.42TFLOPS/W MXFP8 Compute-in-Memory Macro with Adaptive-Preserved-Bit-Width and Serial-Dual-Bit-Sliding Schemes

DS2

X. Wang[1,2], Y. Du[1], T. Jiao[1], D. Wu[1], X. Chen[1], M. Tang[1], Y. Yang[1], Z. Liu[1], A. Guo[1], G. Fu[3], P. Li[3], J. Dong[3], B. Liu[1], X. Liu[1], W. Shan[1], H. Cai[1], G. Sun[4], L. Tong[3], J. Yang[1,2], X. Si[1]

[1]Southeast University, Nanjing, China
[2]National Center of Technology Innovation for EDA, Nanjing, China
[3]Xiaomi, Beijing, China; [4]Peking University, Beijing, China

8:25 AM

30.2 A 12nm 4Mb 104.56-to-137.75TFLOPS/W Charge-Trap Transistor-Based Computing-in-Memory Macro Using Analog-Predict-Digital-Compute for AI Edge Devices

J. Shen[1,2], Z. Zhou*[1,2], W. Zha[1,2], Z. Li[1,2], W. Li[1,2], B. Wang[1,2], J. Zhu[1,2], H. Gao[1,2], Z. Han[1,2], Y. Wang[1,2], L. Wang[3], H. Hu[1,2], Q. Luo[1,2], C. Dou[1,2], M. Liu[1]*

[1]Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China
[2]University of Chinese Academy of Sciences, Beijing, China
[3]Columbia University, New York, NY
*Equally Credited Authors (ECAs)

8:50 AM

30.3 A 22nm 96Mb 50.6-to-90.2TFLOPS/W Non-Linear MLC ReRAM CIM Macro with High-Retention for Mamba/Transformer/CNN

H-H. Hsu[1], W-S. Khwa*[2], Y-K. Yeh[1], C-L. Wu[1], C-Y. Chen[1], Y-C. Huang[1], Y-H. Lin[1], C-F. Chang[1], Y-T. Shao[1], J-C. Tien[1], D-Q. You[1], P-S. Wu[2], B. Zhang[3], R-S. Liu[1], C-C. Hsieh[1], K-T. Tang[1], M-F. Chang[1,2]*

[1]National Tsing Hua University, Hsinchu, Taiwan
[2]TSMC Corporate Research, Hsinchu, Taiwan
[3]TSMC Corporate Research, San Jose, CA
*Equally Credited Authors (ECAs)

9:15 AM

30.4 A 28nm 106.85TOPS/W and 77.68TFLOPS/W CIM Macro with Stage-Wise-Enabled Lossless Compressors Based on Sign-Bit-Embedded Transition-Counting-Lines for Edge-AI Devices

L. Feng, Y. Liu, L. Wu, D. Li, Z. Zhu

Xidian University, Xi'an, China

Break 9:40 AM

10:05 AM

30.5 A 16nm 72kb 120.5TFLOPS/W Versatile-Format Dual-Representation Gain-Cell CIM Macro for General Purpose AI Tasks

J-C. Tien[*1], W-S. Khwa*[*2], L-J. Hsieh[1], T-H. Lou[1], J-C. Bai[1], Y-S. Kao[1], T-H. Hsu[1], M. Tseng[1], H-H. Hsu[1], Y-K. Yeh[1], D-Q. You[1], A. S. Lele[3], B. Crafton[3], B. Zhang[3], P-S. Wu[2], Y-T. Yang[1], C-C. Lo[1], R-S. Liu[1], C-C. Hsieh[1], K-T. Tang[1], M-F. Chang[1,2]*

[1]National Tsing Hua University, Hsinchu, Taiwan
[2]TSMC Corporate Research, Hsinchu, Taiwan
[3]TSMC Corporate Research, San Jose, CA
*Equally Credited Authors (ECAs)

10:30 AM

30.6 A 16Mb 166.8TOPS/W Near-Memory Phase-Domain-Computing Ferroelectric NAND Flash for Approximate Nearest Neighbor Search on Edge Devices

W. Li[*1,2], B. Wang*[*1,2], Z. Zhou[1,2], J. Zhu[1,2], Z. Li[1,2], J. Shen[1,2], W. Zha[1,2], Z. Han[1,2], Y. Wang[1,2], L. Wang[3], H. Hu[1,2], Q. Luo[1,2], C. Dou[1,2], M. Liu[1]*

[1]Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China
[2]University of Chinese Academy of Sciences, Beijing, China
[3]Columbia University, New York, NY
*Equally Credited Authors (ECAs)

10:55 AM

30.7 A 1.2GHz 12.77GB/s/mm² 3D Two-DRAM-One-Logic Process-Near-Memory Chip for Edge LLM Applications

Y. Cao[1,2,3], J. Jiang[1], H. Jiang[3], Q. Zhang[3], X. Liu[2], J. Cheng[2], Z. Han[2], X. Jiang[4], F. Zuo[4], S. Wang[4], F. Bai[4], Y. Guo[4], C. Dou[2], J. Yang[1,2,3], H. Lv[2], Q. Liu[1], M. Liu[1,2]

[1]Fudan University, Shanghai, China
[2]Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China
[3]Zhangjiang Laboratory, Shanghai, China
[4]Xi'an UniIC Semiconductors, Xi'an, China

11:20 AM

30.8 A 16nm, 1Mb, 1-to-8b-Configurable 444.21TOPS/W Fully Digital SRAM Compute-In-Memory Macro for Hybrid SNN-CNN Edge Computing

Y-K. Yeh[*1], J-W. Su*[*2], T-H. Hsu[1], M. Tseng[1], J-C. Tien[1], K-C. Chen[1], C-Y. Yue[1], Y-E. Lin[1], Y-J. Hu[1], L-J. Hsieh[1], J-C. Bai[1], Y-S. Kao[1], T-H. Lou[1], H-H. Hsu[1], D-Q. You[1], S. Shyh-Shyuan[2], W-C. Lo[2], S-C. Chang[1,2], Y-T. Yang[1], C-C. Lo[1], R-S. Liu[1], C-C. Hsieh[1], K-T. Tang[1], M-F. Chang[1]*

[1]National Tsing Hua University, Hsinchu, Taiwan
[2]Industrial Technology Research Institute, Hsinchu, Taiwan
*Equally Credited Authors (ECAs)

11:45 AM

30.9 DS2 A 147TOPS/W, 250TOPS/mm², Fully Synthesizable, Digital Compute-in-Memory Accelerator Supporting INT8×INT8 with Zero-Point Quantization in Intel 18A Technology

A. Agarwal[1], S. K. Hsu[1], M. A. Anders[1], A. Raha[2], D. A. Mathaikutty[3], R. Krishnamurthy[1]

[1]Intel, Hillsboro, OR; [2]Intel, Santa Clara, CA, [3]Intel, Chandler, AZ

Conclusion 12:00 PM

SESSION 31

AI Accelerators

Session Chair: Giuseppe Desoli, *STMicroelectronics, Cornaredo, Italy*
Session Co-Chair: Zhengya Zhang, *University of Michigan, Ann Arbor, MI*

1:30 PM

31.1 A 14.08-to-135.69Token/s ReRAM-on-Logic Stacked Outlier-Free Large-Language-Model Accelerator with Block-Clustered Weight-Compression and Adaptive Parallel-Speculative-Decoding

P. Dong[1,2], Y. Tan[1,2], X. Liu[2], P. Luo[2], Y. Liu[2], D. Pang[2], S. Ma[1,2], X. Huang[1], S-Y. Liu[1], D. Zhang[1,2], Z. Lu[3], L. Liang[2], C-Y. Tsui[1,2], F. Tu[1,2], L. Zhao[4], K-T. Cheng[1,2]

[1]Hong Kong University of Science and Technology, Hong Kong, China
[2]AI Chip Center for Emerging Smart System, Hong Kong, China
[3]Hefei Reliance Memory, Hefei, China
[4]Zhejiang University, Hangzhou, China

1:55 PM

31.2 Revolver: Low-Bit GenAI Accelerator for Distilled-Model and CoT with Phase-Aware-Quantization and Rotation-Based Integer-Scaled Group Quantization

S. Kim, J. Oh, B. Kim, Y. Choi, G. Park, H-J. Yoo

KAIST, Daejeon, Korea

2:20 PM

31.3 A 51.6μJ/Token Subspace-Rotation-Based Dual-Quantized Large-Language-Model Accelerator with Fused Scale-Activation INT Datapath and Rearranged Bit-Slice LUT Computation

B. Liu, Z. Zou, X. Yan, X. Kang, X. Chen, B. Hu, J. Lin, H. Du, J. Yang, X. Si, H. Cai

Southeast University, Nanjing, China

2:45 PM

31.4 VARSA: A Visual Autoregressive Generation Accelerator Using Performance-Scalable Multi-Precision PE-LUT and Grid-Similarity Attention Compression

J. Zhou, H. Li, K. Jiang, Y. Sun, T. Jia

Peking University, Beijing, China

Break 3:10 PM

3:35 PM

31.5 DS2 SoulMate: A 9.8mW Mobile Intelligence System-on-Chip with Mixed-Rank Architecture for On-Device LLM Personalization

S. Hong, J. Choi, J. So, N. Lee, W. Jo, Z. Kalzhan, W. Chin, H-J. Yoo
KAIST, Daejeon, Korea

4:00 PM

31.6 Tri-Oracle: A 17.78μJ/Token Vision-Language Model Accelerator with Token-Attention-Weight Redundancy Prediction

S. Yoo, H. Kim, M. Son, Y. Chen, S. Jeong, J-Y. Kim
KAIST, Daejeon, Korea

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31.7 LUT-SSM: A 99.3TFLOPS/W LUT-Based State-Space Model Accelerator Using Energy-Efficient Element-Wise Layer Fusion and LUT-Friendly Weight-Only Quantization

S. Yoo[1,2], D. Kam*[3], G. Park[4], S. Kwon[1], D. Lee[4], Y. Lee[1]*
[1]Korea Advanced Institute of Science and Technology, Daejeon, Korea
[2]Pohang University of Science and Technology, Pohang, Korea
[3]Ulsan National Institute of Science and Technology, Ulsan, Korea
[4]Naver Cloud, Seongnam, Korea
*Equally Credited Authors (ECAs)

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31.8 A 28nm Speculative-Decoding LLM Processor Achieving 105-to-685μs/Token Latency for Billion-Parameter Models

Y. Wang[1], H. Wang[1], J. Yang[1], Y. Su[1], R. Guo[1], Z. Yue[1], J. Gu[1], S. Wei[1], Y. Hu[1], S. Yin[1,2,3]
[1]Tsinghua University, Beijing, China
[2]Shanghai Artificial Intelligence Laboratory, Shanghai, China
[3]International Innovation Center of Tsinghua University, Shanghai, China

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31.9 DS2 ALPhA-Vision: A Real-Time Always-On Vision Processor with 787μs Face Detection Latency in <5mW

B. Keller[1], R. Venkatesan[1], S. Dai[1], J. Clemons[2], M. Fojtik[3], M. Chang[1], T. Tambe[4], N. Pinckney[2], S. G. Tell[3], Q. Huang[1], S. De Mello[1], B. Khailany[2]
[1]Nvidia, Santa Clara, CA
[2]Nvidia, Austin, TX
[3]Nvidia, Durham, NC
[4]Stanford University, Stanford, CA

Conclusion 5:30 PM

Low-Power Noise-Shaping ADCs

Session Chair: Hajime Shibata, *Analog Devices, Toronto, Canada*
Session Co-Chair: Lucien Breems, *NXP Semiconductors, Eindhoven, The Netherlands*

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32.1 A 98.5dB-SNDR 250kHz-BW 1V-Supply Continuous-Time Zoom ADC with Smart-Tracking and Floating-Tail-Resistor Linearized Gm-C Loop Filter

C. Xing, Y. Cui, S. Pan, Y. Zhong, N. Sun, L. Jie
Tsinghua University, Beijing, China

1:55 PM

32.2 A PVT-Robust Frequency-Scalable Fully Dynamic ΔΣ ADC with Bottom-Plate Level Shift

T. Kaneko[1], H. Ishida[1], Y. Yamaki[1], S. Takehara[1], U-K. Moon[2]
[1]Asahi Kasei Microdevices, Yokohama, Japan
[2]Oregon State University, Corvallis, OR

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32.3 An 85.1dB-SNDR 8MS/s Incremental Pipeline ADC with Dual-Residue-Assisted Exponential Quantization

Z. Wang, B. Li, H. Luo, C. Chu, J. Yang, Y. Wang, X. Tang
Peking University, Beijing, China

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32.4 A 103.9dB-SFDR 83.8dB-SNDR 3MHz-BW Multi-Bit Quadratic-Exponential Noise-Coupled IDSM with High Tolerance to DAC Non-Linearity

Z. Li[1,2], B. Wang[3], M. Guo[1], R. P. Martins[1], S-W. Sin[1]
[1]University of Macau, Macau, China
[2]UM Hetao IC Research Institute, Shenzhen, China
[3]Formula Microelectronics, Shanghai, China

Break 3:10 PM

Time-Varying Circuit Techniques from RF to mm-Wave

Session Chair: Jeremy Dunworth, *Qualcomm Technologies, San Diego, CA*
Session Co-Chair: Wooyeol Choi, *Seoul National University, Seoul, Korea*

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33.1 A 22-to-25GHz CMOS Non-Magnetic Balanced Circulator Achieving at Least 20dB TX-RX Isolation for an Antenna VSWR of 2

H. Deng, E. Shokrolahzade, N. Fakkel, M. Spirito, F. Sebastiano, M. Babaie
TU Delft, Delft, The Netherlands

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33.2 DS2 An Infinite-Loop CMOS-Compatible Isolator Enabled True VSWR-Resilient Power Amplifier for 6G FR3 in Massive MIMO and Phased-Array Systems

M. Ghorbanpoor[1,2], M. Eleraky[2], K. Manetakis[1], P. Nussbaum[1], H. Wang[2]
[1]CSEM, Neuchatel, Switzerland; [2]ETH Zurich, Zurich, Switzerland

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33.3 A 6GHz Quadrature Digital Transmitter Supporting a 1GHz Signal Bandwidth with <-40dB EVM Floor and >55dB Dynamic Range in 28nm CMOS

Y. Li, F. Xie*, Y. Yin, L. Cao, T. Yang, J. Li, H. Xu*
Fudan University, Shanghai, China
*Equally Credited Authors (ECAs)

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33.4 A 4.5-to-7.2GHz Beyond Rail-to-Rail Output SCPA with 27.9dBm P_{out} and 46.2% DE at 5.1GHz Using Periodic Voltage-Pacing Network

B. Yang[1,2], J. Zhou[1], J. Mao[1], X. Luo[1]
[1]Shenzhen University, Shenzhen, China
[2]University of Electronic Science and Technology of China, Chengdu, China

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33.5 A 0.6-to-0.9GHz, 28.06dBm P_{out}, 43.73% SE, 6-Phase Switched-Capacitor Power Amplifier Using In-Cell Digital Waveform Synthesis for the 2nd-, 3rd-, and 4th-Harmonic Suppression

X. Liang[1], B. Yang[1,2], H. Tang[1,2], X. Luo[2]
[1]University of Electronic Science and Technology of China, Chengdu, China
[2]Shenzhen University, Shenzhen, China

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33.6 A Frequency-Translated, 1-to-5GHz Centred, All-Passive, Programmable-Bandwidth, Switched-Capacitor Delay-Line with 6.5-to-8.2dB Delay-Independent Insertion Loss in 65nm CMOS

M. A. Bhat, I. Mondal, Indian Institute of Technology, Kanpur, India

Conclusion 5:35 PM

Integrated Radar and UWB Transceivers from Microwave to Sub-THz

Session Chair: Zhiwei Xu, *Zhejing University, Zhejiang, China*
Session Co-Chair: Wu-Hsin Chen, *Qualcomm, San Diego, CA*

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34.1 DS2 A 128mW 2×4 Radar-on-Chip with Forward-ΔΣ DPLL-Locked Multi-Injection RTWO in 22nm CMOS Enabling ADC-Free Digitization and PS-Free Beamforming Demonstrated in In-Cabin Vital-Sign Monitoring

L. Lou[1], Z. Zhou[1], L. Yuan[1], Y. Long[1], G. Chen[2], X. Li[3], S. Yang[1], H. Cui[1], J. Peng[1], W. Tao[1], J. Deng[1], Y. Hu[1]
[1]University of Science and Technology of China, Hefei, China
[2]National University of Singapore, Singapore, Singapore
[3]Shanghai Jiao Tong University, Shanghai, China

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34.2 Compact, Low-Power 60-and-77GHz 4T/4R Multi-Mode FMCW Radar RFICs in 28nm CMOS

*B-T. *Moon[1], M. *Li[2], J. *Suh[1], M. Lee[1], D. Kim[1], K. Kim[1], G. Park[1], G. Baek[1], B. Yook[1], D. Choi[1], K. Yoo[1], J. Kim[1], T. Yu[1], S. Kang[1], H. Jo[1], J. Son[1], S. Lee[1], P-K. Lau[3], S. I. Lu[3], G. E. Rogers[3], A. Jain[3], J. Wang[2], V. Ariyarathna[2], W. J. Kim[2], O. Eliezer[2], G. Feygin[2], W. Zhou[2], K-J. Moon[1], J. Chung[1], W. Lee[1], S. Kim[1], J. Kim[1], J. Lee[1], T. Kim[1], S. Kim[1], Y. Lee[1], Y. H. Jang[2], S. K. Rayudu[3], S. Chien[3], Y. Chen[3], H. Lim[1], K. Kang[1], S. Lee[1], J. Lee[1], J. Bae[1], H-G. Seok[1], P. Dayal[2], W. Wu[3], H-C. Park[1], J. Hur[3], S. Yoo[1], C-H. Park[1], J. Kim[1]*
[1]Samsung Electronics, Hwaseong, Korea
[2]Samsung Electronics, San Diego, CA;[3]Samsung Electronics, San Jose, CA
*Equally Credited Authors (ECAs)

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34.3 DS2 A 234-to-252GHz Dual-Polarized Transceiver Using Antenna-in-Package Technologies for Cross-Polarimetric Sensing

X. Chen[1], G. C. Dogiamis[2,3], R. Han[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]Intel, Chandler, AZ; [3]Deca Technologies, Tempe, AZ

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34.4 DS2 A 1.6-to-3.8GHz Reconfigurable FMCW Radar SoC with 81.5% Relative-Bandwidth PLL for Real-Time Life Detection in Disaster Response

R. Fu[1], L. Shi*[1], F. Cai[1], Y. Yang[1], H. Lei[1], Z. Fu[1], Y. Xu[1], P. Wang[1], Z. Li[1], S. Wang[1], J. Jiao[1], D. Liang[1], L. Wu[1,2], G. Zhang[3], N. Du[3], Z. Wang[1], Y. Gu[1], X. Ye[3], X. Fang[1], W. Zhao[1,2], H. Zhang[1,2]*
[1]Beihang University, Beijing, China
[2]Tianmushan Laboratory, Hangzhou, China
[3]Beijing Institute of Technology, Beijing, China
*Equally Credited Authors (ECAs)

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34.5 DS2 A 0.0523mm² 11.4mW IEEE 802.15.4a/z/ab Compatible Aliasing-Suppressing All-Digital IR-UWB Transmitter Featuring Comb-Notched Maximally Flat Amplitude Spectral Shaping

J. Son, M. Park, C. Park, K. Lee, J-H. Yoon, J. Lee, M. Song
Daegu Gyeongbuk Institute of Science and Technology, Daegu, Korea

Break 3:15 PM

Low Power Wireless Transceivers for Localization and Communications

Session Chair: Konstantinos Manetakis, *CSEM, Neuchâtel, Switzerland*
Session Co-Chair: Julian Tham, *Infineon, San Jose, CA*

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35.1 CANCEL: A Cancellation-Aided Ambient IoT Nanopowered Communication System for Energy-Limited Tags

H. Abolmagd[1,2], S-K. Kuo[3], M. N. Hasan[1], S. Kadaveru[3], A. Ghorbani Nejad[1], M. Dunna[3], A. Khorami[1], Y. Yu[3], D. Bharadia[3], P. Mercier[3], S. Shekhar[1]

[1]University of British Columbia, Vancouver, Canada
[2]now with Nokia, Ottawa, Canada
[3]University of California, San Diego, CA

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35.2 A 20mg Battery-Free Crystal-Less Miniaturized TX System for Flying Insects Localization with 1.45km Range

Y. Shen, S. Young, D. Komma, R. Strohman, R. Narasimha, J. Chang, A. Bejarano-Carbo, Y. Wang, G. Tao, H-S. Kim, D. Blaauw

University of Michigan, Ann Arbor, MI

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35.3 A 0.052mm² Blocker-Tolerant Non-Uniform Current Sub-Sampling Receiver with a Discrete-Time FIR/IIR Filter Enabling 56dB Rejection in 28nm CMOS

M. Ayesh[1,2], M-W. Chen[2]

[1]now with Marvell, Irvine, CA
[2]University of Southern California, Los Angeles, CA

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35.4 A NearLink 2.0 Compliant Dual-Band RF Transceiver for Smart Wireless Personal Audio Applications

R. Yu[1], S. Liu[1], X. Chen[1], T. Zhang[1], W. K. Chan[1], D. Hu[1], H. Yu[1], W. Yao[1], T. T. Yeo[1], P. Wu[2], X. Zhao[2], Z. Guo[2]

[1]Huawei Technologies, Shenzhen, China
[2]HiSilicon Technologies, Shanghai, China

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35.5 DS2 Fully Integrated Backscattered WiFi 802.11b Transmitter with Active Harmonics and Image Rejection for 30dB IRR and 36dB HRR at 0.88μW

R. Yang, K. Ali, M. Alioto

National University of Singapore, Singapore, Singapore

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SESSION 36

Neural and Biomedical Interfaces

Session Chair: Mahsa Shoaran, EPFL, *Geneva, Switzerland*
Session Co-Chair: Carolina Mora Lopez, *imec, Leuven, Belgium*

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36.1 DS2 ReFIND: A Resolution-Reconfigurable Bio-Signal Classification SoC Enabling >10× Savings in AFE Power per Channel

A. Pandey[1], I-T. Lin[1], D. Vaish[1], A. Rammohan[1], S. Bhat[1], J. Pinkenburg[1], R. Muller[1,2]
[1]University of California, Berkeley, CA
[2]Weill Neurohub, Berkeley, CA

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36.2 DS2 A Neural Interface SoC for Smart Glasses with Low-Power Neural Commanding and Efficient LoRA-Enabled On-Chip Learning

Z. Zhong[1], H. Yu*[1], W. McGarry[1], Y. Wei[2], J. Gu[1]*
[1]Northwestern University, Evanston, IL
[2]Texas Instruments, Dallas, TX
*Equally Credited Authors (ECAs)

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36.3 A 16.4nJ/Class Patient-Independent Prototype-Based Spatio-Temporal CNN Processor with Forward-Inference-Based Adaptation for Robust and Low-Latency Seizure Detection

Y. Wang[1], L. Lin[1], J. Yoo[2], J. Li[1]
[1]Southern University of Science and Technology, Shenzhen, China
[2]Seoul National University, Seoul, Korea

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36.4 ANP-OT: A 0.17nW/Synapse 0.46pJ/SOP Neuromorphic Olfactory Processor with On-Chip Transfer Learning for Non-Invasive Cross-Hospital Cross-Pulmonary-Disease Diagnosis

D. Huo[1], Z. Cheng*[1], J. Zhang[1], Y. Jiang[2], L. Zhang[3], H. Wang[3], N. Ma[2], Z. Huang[2], M. Lin[2], Y. Zhao[3], Z. Wang[1], K-T. Tang[4], H. Chen[1]*
[1]Tsinghua University, Beijing, China
[2]Beijing Tsinghua Changgung Hospital, Beijing, China
[3]Hebei Medical University Third Hospital, Shijiazhuang, China
[4]National Tsing Hua University, Hsinchu, Taiwan
*Equally Credited Authors (ECAs)

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36.5 A 185.6dB-FOM$_{DR}$ 180.3dB-FOM$_{SNDR}$ 10.64-NEF NS-SAR-ADC with Calibration-Free 2nd-Order kT/C-Noise Shaping for Wearable ExG Acquisition

G. Kim, K. Park, M. Lee, J. Wie, S. Jeong, Y. Shin, K. Lee, J-H. Yoon, M. Song, J. Lee
Daegu Gyeongbuk Institute of Science and Technology, Daegu, Korea

Break 3:15 PM

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36.6 DS2 Sparsity-Aware Neural Interface with CIM-Based Predictive Focused Sampling for Hotspot Spike Tracking

H. Wu[*1], *F. Tian*[*2], *J. Chen*[1], *Z. Liao*[1], *H. Zhang*[1], *X. Liu*[1], *W. Zou*[1], *S. Cheng*[1], *Z. Zhang*[3], *J. Xu*[4], *C-Y. Tsui*[2], *K-T. T. Cheng*[2], *J. Yang*[1], *M. Sawan*[1]
[1]Westlake University, Hangzhou, China
[2]Hong Kong University of Science and Technology, Hong Kong, China
[3]Institute of Semiconductors of the Chinese Academy of Sciences, Beijing, China
[4]Soochow University, Suzhou, China, *Equally Credited Authors (ECAs)

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36.7 A 90.7%-Efficiency Hybrid Optogenetic Stimulation System with Sub-Threshold Electrical Stimuli Achieving 70.6% Optical Energy Saving

J. Kang[1], *H. Roh*[2], *K. Eom*[1], *H-S. Lee*[1], *H. Chon*[1], *M. Im*[2], *H-M. Lee*[1]
[1]Korea University, Seoul, Korea
[2]Korea Institute of Science and Technology, Seoul, Korea

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36.8 An 80×80μm²/Pixel 55.48dB-Wide-DR 400-Pixel Subretinal Prosthesis SoC with Power-Aware Light Adaptation and Charge-Recycling Local Dynamic Supply

K. Eom[1], *H-S. Lee*[1], *M. Kim*[2], *M. Im*[2], *H-M. Lee*[1]
[1]Korea University, Seoul, Korea
[2]Korea Institute of Science and Technology, Seoul, Korea

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36.9 A CMOS Neural Probe with 1280 Electrodes and 88 Emission Sites Featuring Thermo-Optic Switching and On-Chip Calibration for Dual-Wavelength Optogenetics

*X. Yang**, *P. Neutens**, *A. Humblet*, *C. Sawigun*, *J. O'Callaghan*, *T. Geurts*, *Z. Li*, *Y. Gubin*, *K. De Munck*, *H. A. C. Tilmans*, *A. De Proft*, *B. Dutta*, *C. Mora Lopez*
imec, Heverlee, Belgium, *Equally Credited Authors (ECAs)

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36.10 A 43.8-to-662.0μW 27.5-to-878.9fps Frame-Rate-Scalable Duty-Cycled Electrical Impedance Tomography System with MIMO Current-Balancing IA

H. Choi[*1], *G. Yun*[*1], *J-H. Suh*[2], *S. Park*[1], *D. Yi*[1], *S. Ha*[3], *M. Je*[1]
[1]KAIST, Daejeon, Korea; [2]University of California, San Diego, CA
[3]New York University Abu Dhabi, Abu Dhabi, United Arab Emirates
*Equally Credited Authors (ECAs)

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36.11 DS2 A 0.62μW/sensor 82fps Time-to-Digital Impedance Measurement IC with Unified Excitation/Readout Front-End for Large-Scale Piezo-Resistive Sensor Array

J. Li[1,2], *Q. Zhang*[2], *S. Ha*[2,3], *A. Demosthenous*[2], *D. Jiang*[2], *Y. Wu*[2]
[1]University of Bristol, Bristol, United Kingdom
[2]University College London, London, United Kingdom
[3]New York University Abu Dhabi, Abu Dhabi, United Arab Emirates

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SESSION 37

Memory Interface

Session Chair: Dongkyun Kim, *SK hynix, Icheon, Korea*
Session Co-Chair: Hye-Ran Kim, *Samsung Electronics, Anyang, Korea*

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37.1 A 72Gb/s/pin Single-Ended Driver-Cooperative Coded PAM3 Transceiver with Asymmetric Data-Dependent Equalization and Bias-Peaking for Chiplets and Memory Interfaces

H. Wu, X. Cheng, Y. Zhang, X. Luo, Z. Li, W. Wu, Q. Pan

Southern University of Science and Technology, Shenzhen, China

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37.2 A 47.0Tb/s/mm 112Gb/s/pin PAM4 Single-Ended Transceiver Featuring 4-Aggressor Crosstalk Cancellation and Supply-Noise Tolerance for Short-Reach Memory Interfaces

Q. Liu[1], Y. Hui[1], Y. Nong[1], H. Ma[1], Y. Xu[1], H. Hu[1], J. Zhu[1], Q. Wang[2], L. Wang[2], L. Du[1,3], Y. Du[1,3]

[1]Nanjing University, Nanjing, China
[2]T-Head (Shanghai) Semiconductor, Shanghai, China
[3]Interdisciplinary Research Center for Future Intelligent Chips (Chip-X), Suzhou, China

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37.3 A 2nm All-Digital 14.4Gb/s/pin LPDDR6 PHY with Quarter-Rate Clocking Architecture and Multi-Level FIFO-Based Speculative DFE

Y. Choi, D. Kim, M. Kim, S. Lee, H. Kang, G. Lee, Y. Kim, S. Kang, H. Cho, B. Kang, K. Lee, J. Song, J. Choi, S. Yi, B. Koo, K. Chae, H-G. Rhew

Samsung Electronics, Yongin, Korea

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37.4 A 100Gb/s, 1.92pJ/b Aggregate 4-Lane Single-Ended NRZ Transceiver with 15dB Far-End Crosstalk Cancellation via On-Chip Feature Extraction and Classification in 16nm FinFET

X. Lin, R. Javadi, B. Bose, T. Anand

Oregon State University, Corvallis, OR

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37.5 A 16Gb/s/pin 0.51pJ/bit Single-Ended NRZ Transceiver with Distributed Dual-Loop VDDQ Ripple Compensation and Dynamic Clock Duty-Cycle Calibration for Memory Interfaces

Y. He[1], Y. Luo*[1], Y. Wang*[1], T. Yi[2], C. Jiang[1], C. Chen[1], Q. Liu[1], M. Liu[1], W. Jiang[1]*

[1]Fudan University, Shanghai, China
[2]ZhangJiang Laboratory, Shanghai, China
*Equally Credited Authors (ECAs)

Break 3:15 PM

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37.6 A 0.092pJ/b and 7.7fJ/b/dB Cross-Self-Referenced Slope-Sampling Receiver with Long-Tail ISI Robustness for Next-Generation Low-Power Memory Interfaces

K-S. Lee, C. Han*, J-H. Chae*

Kwangwoon University, Seoul, Korea
*Equally Credited Authors (ECAs)

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37.7 A 12.8Gb/s Parallel Receiver with a One-Way Self-Training Scheme for Equalizing ISI and Reflections in Multi-Drop Memory Interfaces

J-W. Moon[1], T. Kim[1], M. Kim[1], H. Seong[1], J. Lee[1], J. Park[1], D. Park[1], J. Lee[1], J-J. Park[2], C. Yoon[2], J-Y. Sim[1], S-K. Lee[1]

[1]Pohang University of Science and Technology, Pohang, Korea
[2]Samsung Electronics, Hwaseong, Korea

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37.8 A 0.87pJ/b 17Gb/s/pin Parallel Receiver with a Local DQS Recovery for Supply-Noise-Tolerant DQS Distribution in High-Performance NAND Flash Interfaces

B-C. Kim[1], K. Lee[1], D. Park[1], J-J. Park[2], C. Yoon[2], J-Y. Sim[1], S-K. Lee[1]

[1]Pohang University of Science and Technology, Pohang, Korea
[2]Samsung Electronics, Hwaseong, Korea

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37.9 A 14Gb/s/pin 0.163pJ/b DQ Receiver for HBM with Baud-Rate Phase Tracking Loop Supporting Background Offset Calibration

J. Lee[1], H-J. Shin[1], H-G. Ko[2], K. Park[1]

[1]Yonsei University, Seoul, Korea
[2]ONEsemiconductor, Gyeonggi, Korea

Conclusion 5:15 PM

Powering the Future of AI, HPC, and Chiplet Architectures: From Dies to Package and Rack

Organizers: **Xin Zhang,** *IBM T. J. Watson Research Center, Yorktown Heights, NY*
Kazuki Fukuoka, *Renesas Electronics, Tokyo, Japan*

Co-Organizers: **Ping-Hsuan Hsieh,** *National Tsing Hua University, Hsinchu, Taiwan*
Monodeep Kar, *IBM T. J. Watson Research Center, Yorktown Heights, NY*
Srividhya Venkataraman, *AMD, Santa Clara, CA*
Rinkle Jain, *Nvidia, Santa Clara, CA*
Nicolas Butzen, *Intel, Hillsboro, OR*

Champions: **Meng-Fan Chang,** *National Tsing Hua University, Hsinchu, Taiwan*
Makoto Nagata, *Kobe University, Kobe, Japan*

As AI, HPC, and chiplet-based architectures push the boundaries of performance and integration, intelligent and efficient power management becomes more critical than ever. This forum will explore state-of-the-art power delivery techniques across the full compute stack—from die and package to system and rack levels.

Topics will include power conversion and integrity trends in data-center processors, package-integrated voltage regulators, energy-efficient control strategies, and power converter topologies. Advances in integrated power devices, package-embedded passive technologies, and power integrity optimization for high-bandwidth DRAM will also be discussed. The forum will address emerging challenges posed by AI, HPC and chiplet architectures, as well as the impact of these innovations on system efficiency, scalability, and sustainability.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Xin Zhang,** *IBM T. J. Watson Research Center, Yorktown Heights, NY*
8:25 AM	**Integrated Voltage Regulator Solutions to Enable 5kW GPUs** **Kaladhar Radhakrishnan,** *Intel, Chandler, AZ*
9:15 AM	**Power Delivery Trends and Demands in Data-Center AI Processors** **Houle Gan,** *Google, Sunnyvale, CA*
10:05 AM	Break
10:20 AM	**Energy Efficiency and Power Management Techniques for AI Accelerators** **Luca Benini,** *Università di Bologna, Bologna, Italy, ETH Zürich, Zürich, Switzerland*
11:10 AM	**3D Vertical Power Delivery for AI and Chiplet Systems** **Yan Lu,** *Tsinghua University, Beijing, China*
12:00 PM	Lunch
1:20 PM	**Progress and Scaling in Integrated Power Devices** **Sameer Pendharkar,** *TI, Dallas, TX*
2:10 PM	**Integrated Magnetics for Datacenter Applications** **Maeve Duffy,** *University of Galway, Galway, Ireland*
3:00 PM	Break
3:15 PM	**Packaging-Aware Design and Optimization of HBM Power Delivery in AI Platforms** **Daihyun Lim,** *Samsung DSA, San Jose, CA*
4:05 PM	**Powering UP Heterogeneously Integrated Multi-Die / Multi-Chiplet Systems** **Farhana Sheikh,** *Intel, Hillsboro, OR*
4:55 PM	Closing Remarks

The Race for 6G FR3 (7-24GHz): From Network Deployment to System Integration and Breakthrough Technology

Organizers: **Wu-Hsin Chen,** *Qualcomm, San Diego, CA*
Yuanjin Zheng, *Nanyang Technological University, Singapore, Singapore*

Co-Organizers: **Chi-Hang (Ivor) Chan,** *University of Macau, Taipa, Macau*
Konstantinos Manetakis, *CSEM, Neuchâtel, Switzerland*
Negar Reiskarimian, *Massachusetts Institute of Technology, Cambridge, MA*
Yun Wang, *Fudan University, Shanghai, China*

Champions: **Danielle Griffith,** *Texas Instruments, Dallas, TX*
Matteo Bassi, *Infineon Technologies AG, Villach, Austria*

As we are finally entering the 6G era, this forum will provide an overview of the challenges and opportunities for the 6G FR3 (7 to 24 GHz). It will delve into system-level considerations, front-end module architectures, spectrum sharing and interference cancellation, offering insights into the next generation of cellular technology. Additionally, the forum will address design techniques for FR3, such as direct ADC sampling, PA linearity and efficiency improvement with Doherty architecture or digital predistortion. It will also discuss process technologies for highly efficient FEMs across different parts of the FR3 bands, evaluating the pros and cons of candidate technologies like GaN-Si. Other critical emerging technologies, such as joined communication and sensing,and ambient IoT, will also be covered. Finally, the use of AI/ML to enhance FR3 network performance will also be explored.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Wu-Hsin Chen,** *Qualcomm, San Diego, CA*
8:25 AM	**System Consideration and Coexistence with Other Incumbent Services** **Shawn Tsai,** *Mediatek, San Diego, CA*
9:10 AM	**FR3 FEM Architectures: Heterogeneous Integration from Antenna to RF Circuitry** **Li Liu,** *Qualcomm, San Diego, CA*
9:55 AM	Break
10:10 AM	**Spectrum Sensing, Sharing and Interference Cancellation Technologies** **Arun Natarajan,** *Yale, New Haven, CT*
10:55 AM	**FR3 System Analysis, Testbed and Hardware Challenges** **Gary Xu,** *Samsung, Plano, TX*
11:40 AM	**6G FR3 RF Front-End Modules and Power Amplifiers for Mobile Applications** **Florinel Balteanu,** *Skyworks, Irvine, CA*
12:25 PM	Lunch
1:40 PM	**Direct RF Sampling ADCs for FR3** **Junhua Shen,** *Analog Devices, Wilmington, MA*
2:25 PM	**Exploration of 6G FR3 for Coverage, Capacity, and Sensing in the Edge AI Era** **Kenichi Okada,** *Institute of Science Tokyo, Tokyo, Japan*
3:10 PM	Break
3:25 PM	**Ambient IoT: From Concept to Practicality** **David Wentzloff,** *Everactive/UMICH, Ann Arbor, MI*
4:10 PM	**Site-Specific MIMO Channel Optimization in FR3** **Sofie Pollin,** *Leuven/IMEC, Leuven, Vlaams-Brabant, Belgium*
4:55 PM	Closing Remarks

Analog for AI and AI for Analog: What the Analog/RF People Can Do and Leverage in the AI Era

Organizers: **Jiayoon Ru,** *Peking University, Beijing, China*
Vanessa Chen, *Carnegie Mellon University, Pittsburgh, PA*

Co-Organizers: **Masoud Babaie,** *Delft University of Technology, Delft, The Netherlands*
Taiyun Chi, *Rice University, Houston, TX*
Jun Yang, *Southeast University, Nanjing, China*
Didem Turker Melek, *Cadence Design Systems, San Jose, CA*

Champions: **Mingoo Seok,** *Columbia University, New York, NY*
Kostas Doris, *NXP, Eindhoven, The Netherlands*

As AI advances rapidly, digital circuits such as GPUs work at its foundation, yet analog and mixed-signal circuits remain essential to build AI infrastructure and complement AI computing. At the same time, AI starts to influence the way ICs are modeled, designed, optimized, and packaged. The forum intends to bring the analog community together for a one-stop shop to have a comprehensive understanding and discussion of our impact on AI, and the impact of AI on our jobs and potentially on the way we solve analog problems. By bridging these perspectives, the forum will explore challenges and opportunities for analog/RF/mixed-signal engineers and researchers to shape next-generation AI systems and to leverage AI for improving our design and productivity.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Jiayoon Ru,** *Peking University, Beijing, China*
8:25 AM	**Analog for AI and AI for Analog: Enabling Next-Generation AI Datacenters** **Tom Gray,** *NVIDIA, Durham, NC*
9:10 AM	**What Role Can Analog Computation Play in Next-Generation AI Systems** **Naveen Verma,** *Princeton University, Princeton, NJ and EnCharge AI, Santa Clara, CA*
9:55 AM	Break
10:10 AM	**Algorithm Architecture Co-Design for Analog In-Memory Computing** **Hsinyu (Sidney) Tsai,** *IBM, San Jose, CA*
10:55 AM	**Open-Source AI for Analog Correction: From RF Power Amplifiers to Energy-Efficient Silicon** **Chang Gao,** *Delft University of Technology, Delft, The Netherlands*
11:40 AM	**Challenges in AI-Based Analog Design** **Behzad Razavi,** *UCLA, Los Angeles, CA*
12:25 PM	Lunch
1:40 PM	**State-of-the-art Microwave Device Modeling Enabled by Artificial Intelligence and Machine Learning** **Jianjun Xu,** *Keysight Technologies, Santa Rosa, CA*
2:25 PM	**Toward Agile and Intelligent Analog/RF IC Design Automation** **David Pan,** *UT Austin, Austin, TX*
3:10 PM	Break
3:25 PM	**AI-Empowered Analog/RF IC Design** **Ye Lu,** *Fudan University and RFIC-GPT, Shanghai, China*
4:10 PM	**Handling the Design Complexities of 2D, 2.5D, and 3D Microsystem Assemblies Possessing Heterogeneous Functionality Using AI-Based EDA Technology** **John Damoulakis,** *Cadence Design Systems, San Jose, CA*
4:55 PM	Closing Remarks

Calibration and Dynamic Matching Techniques for High-Performance Data Converters

Organizers: **Lucien Breems,** *NXP Semiconductors, Eindhoven, The Netherlands*
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Digital assistance through calibration and dynamic matching is a key enabler in modern data converters, enhancing robustness, reducing analog complexity through digital processing, and enabling extreme levels of bandwidth and resolution. These matching techniques correct a wide range of errors — including offset, gain mismatches, dynamic variations, frequency-dependent distortions, and time skew — to ensure high-precision operation. This forum presents a comprehensive overview of calibration strategies and dynamic matching algorithms employed across various data converter architectures: high-speed ADCs, high-speed DACs, continuous-time pipeline ADCs, noise-shaping ADCs, and time-domain ADCs. Looking ahead, the integration of AI and machine learning into calibration workflows holds promise for even greater adaptability and performance.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Lucien Breems,** *NXP Semiconductors, Eindhoven, The Netherlands*
8:25 AM	**Data Converter Calibration: Motivation, Evolution, and General Aspects** **Boris Murmann,** *University of Hawai'i, Honolulu, Hawaii*
9:15 AM	**Background Calibration of High-Speed Pipelined ADCs: Methods, Limitations and Practical Considerations** **Huseyin Dinc,** *Analog Devices, Durham, NC*
10:05 AM	Break
10:20 AM	**High-Linearity in Delta-Sigma ADCs Using DEM, Calibration, and Architectural Innovation** **Maurits Ortmanns,** *University of Ulm, Ulm, Germany*
11:10 AM	**Ensuring Robustness in MASH / Continuous-Time Pipeline ADCs: Necessity of Calibration** **Mitsuya Fukazawa,** *Renesas, Tokyo, Japan*
12:00 PM	Lunch
1:20 PM	**Calibration for High-Speed, High-Resolution DACs** **Gabriele Manganaro,** *Mediatek, Woburn, MA*
2:10 PM	**Machine Learning-Based Calibration of Analog-to-Digital Converters** **Maarten Molendijk,** *NXP Semiconductors, Eindhoven, The Netherlands*
3:00 PM	Break
3:15 PM	**Calibration Techniques for High-Speed Time-Interleaved Time-Domain ADCs** **Sam Palermo,** *Texas A&M University, College Station, TX*
4:05 PM	**Panel Discussion** **Kostas Doris,** *NXP Semiconductors, Eindhoven, The Netherlands*
4:55 PM	Closing Remarks

Circuits for Optical Subsystems: Communications and Beyond

Agenda

Time:	Topic:
8:00 AM	Breakfast
8:25 AM	**Introduction by Chair** ***Daniel Friedman,*** *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*
8:30 AM	**Introduction to Optical Communication Systems: From VCSELs to Photonics to Coherent Solutions** ***Peter Ossieur,*** *imec, Ghent, Belgium*
10:00 AM	Break
10:30 AM	**VCSEL-Based Solutions: Components, Circuits, and Integration** ***Enrico Temporiti,*** *Marvell, Pavia, Italy*
12:15 PM	Lunch
1:20 PM	**Silicon Photonics-Based Solutions: Components, Circuits, and Integration** ***Firooz Aflatouni,*** *University of Pennsylvania, Philadelphia, PA*
2:50 PM	Break
3:20 PM	**Emerging Optical Applications and Circuit Approaches** ***Ali Hajimiri,*** *California Institute of Technology, Pasadena, CA*
4:50 PM	Conclusion

Introduction

Optical subsystems are taking on growing importance, going beyond traditional critical roles in long- and medium-distance high data rate communication applications toward ever-expanding use cases within compute racks as well as in emerging optical array applications. Circuit and integration techniques supporting optical designs are critical enablers of this growth. Progress in this area is even more critical given the challenges facing increasing per-lane data rates for electrical designs coupled with the seemingly insatiable growth in demand for bandwidth to support data center and AI accelerator workloads. This short course is designed to explore these interface circuits. The first presentation provides an introduction to optical communication subsystems, including a discussion of coherent designs. The second lecture focuses on VCSEL-based solutions, including reviewing optical component characteristics, circuit techniques, and packaging strategies enabling integration in ultra-high bandwidth contexts. The third lecture explores silicon photonics-based design, again reviewing critical system components, here including source lasers, modulators, couplers, detectors, and integration strategies. Finally, the last lecture introduces emerging applications for optical subsystems, including optical phased array-based designs.

8:30 AM

SC1: Introduction to Optical Communication Systems: From VCSELs to Photonics to Coherent Solutions

Peter Ossieur, *imec, Ghent, Belgium*

This presentation starts off with a thorough introduction to optical link architectures and their important figures of merit, covering intensity modulated, direct detect, and coherent transmission approaches. Then, as a first means to realize an optical link, direct modulation relying on VCSELs is addressed. This is followed by external modulation with particular focus on Silicon Photonics and InP platforms. The lecture ends with a detailed treatment of dual-polarization, IQ modulation and coherent detection.

Peter Ossieur is a scientific director at imec leading optical interconnect R&D, and holds a part time position as professor of high-speed opto-electronics at Ghent University, Belgium. Prof. Ossieur obtained the PhD degree from Ghent University, Belgium, 2005, where he continued to work as a postdoctoral researcher until 2009. From 2009 till 2017, he worked at Tyndall National Institute, Ireland, eventually as Senior Staff Researcher. His research interests are focused upon high-speed electronic and photonic integrated circuits targeting optical and electrical transceivers. He has authored or co-authored over 200 conference and journal publications. Currently, he is serving on the ISSCC wireline subcommittee.

10:30 AM

SC2: VCSEL-Based Solutions: Components, Circuits, and Integration

Enrico Temporiti, *Marvell, Pavia, Italy*

This lecture explores VCSEL-based solutions for short-reach optical interconnects, essential for intra-datacenter connectivity and increasingly critical in AI architectures. After reviewing key optical components, we examine high-speed driver circuits and integration strategies for compact, scalable transmitters. The talk progresses from fundamentals to state-of-the-art advancements, concluding with opportunities and challenges amid relentless bandwidth growth and evolving datacenter demands.

Enrico Temporiti earned his MSc in Electronic Engineering from the University of Pavia in 1999. In 2000 he joined STMicroelectronics, working in R&D and product development. Since 2019 he has been with Marvell, where he serves as Sr. Director of Engineering, leading electro-optical PHY development.

1:20 PM

SC3: Silicon Photonics-Based Solutions: Components, Circuits, and Integration

Firooz Aflatouni, *University of Pennsylvania, Philadelphia, PA*

In this lecture, monolithic and hybrid electronic-photonic integration approaches are discussed and design approaches for key passive and active photonic devices such as single-mode and multi-mode waveguides, couplers, delay-lines, photodiodes, and modulators are presented. Laser sources and packaging of silicon photonic chips with lasers are discussed and typical noise sources in electronic photonics systems are introduced. Finally, examples of electronic-photonic systems such as optical interconnects using wavelength-division-multiplexing for data-centers and photonic compute modules are presented.

Firooz Aflatouni received the Ph.D. degree in Electrical Engineering from the University of Southern California. He was a post-doctoral scholar in the Department of Electrical Engineering at Caltech before joining the University of Pennsylvania where he is a Professor of Electrical and Systems Engineering. Firooz received the Bell Labs Prize in 2020, the ONR Young Investigator Program Award in 2019, the NASA Early-Stage Innovation Award in 2019, and the 2015 IEEE Benjamin Franklin Key Award. He is a fellow of Optica, and has served as a Distinguished Lecturer of the SSCS and on several IEEE conference program committees.

3:20 PM

SC4: Emerging Optical Applications and Circuit Approaches

Ali Hajimiri, *California Institute of Technology, Pasadena, CA*

In this presentation, we will discuss emerging optical applications and novel solutions enabling the co-integration of photonics and electronics. We will explore free-space applications such as imaging and projection, as well as the requirements and recent progress in photonic solutions for squeezed light. We will then introduce a subtractive photonic platform that leverages standard CMOS electronic circuits, utilizing the dielectric between metal lines as optical components capable of guiding light at visible and infrared wavelengths.

Ali Hajimiri is Bren Professor of Electrical Engineering and Medical Engineering at California Institute of Technology (Caltech) where he is the Director of the Microelectronics Laboratory, and the Co-Director of the Space Solar Power Project. He is a Fellow of National Academy of Inventors and a Fellow of the IEEE. Hajimiri holds close to 200 issued patents in the field of high-speed and high-frequency integrated circuits for sensors, photonics, biomedical devices, and communication systems. He co-founded Axiom Microdevices Inc. in 2002, which was later acquired by Skyworks Inc. in 2009. He is a recipient of several prestigious awards, including the Feynman Prize for Excellence in Teaching.

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HOW TO REGISTER FOR ISSCC

Online: This is the only way to register and will give you immediate email confirmation of your events. Go to the ISSCC website at www.isscc.org and select the link to the Registration website.

Payment Options: Immediate payment can be made online via credit card. **Registrations received without full payment will not be processed until payment is received at YesEvents.** Please read the instructions on the Registration website.

COVID 19 PROTOCOLS

The health and safety of our conference attendees is our top priority. The ISSCC 2026 conference Organizing Committee remains vigilant in monitoring the COVID-19 pandemic. The conference will follow CDC and State of California guidelines. ISSCC is planned as an in-person event but it also has an online offering. We look forward to you joining us in San Francisco, CA. If you don't feel comfortable participating in large gatherings, or if your organization has travel restrictions, we encourage you to join us online.

MASKS, VACCINATION, SANITIZERS

Masks help slow the spread of the virus. They help to protect the medically vulnerable and those unable to get vaccinated. In San Francisco there are no longer masking requirements for most people. People may choose to wear masks, even when they are not required. Respect the choices others make for their health.

Currently, proof of vaccination is no longer required in meetings in San Francisco. We will be monitoring that regulation and the ISSCC website will be updated as regulations change.

Hand sanitizing lotion will be available throughout the hotel and at the Registration desk.

REGISTRATION DESK HOURS:

Saturday, February 14:	**4:00 pm to 7:00 pm**
Sunday, February 15:	**7:00 am to 8:30 pm**
Monday, February 16:	**6:30 am to 4:00 pm**
Tuesday, February 17:	**8:00 am to 4:00 pm**
Wednesday, February 18:	**8:00 am to 4:00 pm**
Thursday, February 19:	**7:00 am to 2:00 pm**

Students must present their Student ID
at the Registration Desk to receive the student rates.

Those registering at the IEEE Member rate
must login to their IEEE membership during registration.

Deadlines: The deadline for registering at the Early Registration rates is 12:00 Midnight EST **Sunday January 11, 2026.** After January 11th, and before 12:00 Midnight EST **Monday January 26th, 2026,** registrations will be processed **at the Late Registration rates. After January 26th, you must register at the on-site rates.** You are urged to register early to obtain the lowest rates and ensure your participation in all aspects of ISSCC.

Cancellations/Adjustments: Prior to 12:00 Midnight EST **Monday January 26, 2026,** conference registration can be cancelled. Fees paid will be refunded (less a processing fee of $75). Send an email to the registration contractor at ISSCCinfo@yesevents.com to cancel or make other adjustments.

No refunds will be made after 12:00 Midnight EST January 26th, 2026. Paid registrants who do not attend the conference will have access to the on-demand material.

IEEE MEMBERSHIP SAVES ON ISSCC REGISTRATION

Take advantage of significantly reduced ISSCC fees by using your IEEE membership number. Additional savings are available for members of the IEEE Solid-State Circuits Society. If you're an IEEE member and have forgotten your member number, simply phone IEEE at 1(800) 678-4333 (US and Canada) or +1 732-981-0060 (all other regions) and ask. IEEE membership staff will take about two minutes to look up your number for you. If you come to register on site without your membership card, you can phone IEEE then, too. Or you can request a membership number look-up online at https://supportcenter.ieee.org. If you're not an IEEE member, consider joining before you register to save on your fees. Join online at www.ieee.org/join any time and you'll receive your member number by email. When joining IEEE you can also select a Solid-State Circuits Society (SSCS) membership, which more than pays for itself by giving you an additional $30 off the registration fee among other benefits.

SSCS MEMBERSHIP
A VALUABLE PROFESSIONAL RESOURCE FOR YOUR CAREER GROWTH

Stay Current! Get Connected! Invest in your Career! Membership in the Solid-State Circuits Society offers you the chance to explore solutions within a global community of colleagues in our field. Membership extends to you the opportunity to grow and share your knowledge, hone your expertise, expand or specialize your network of colleagues, advance your career, and give back to the profession and your local community.

SSCS MEMBERSHIP DELIVERS:

- Tools for Career growth
- Educational development
- Networking with peers
- Recognition for your achievements
- Leadership opportunities

We invite you to join or renew today to participate in exclusive educational events, access to leading research and best practice literature, and start your own career legacy by mentoring students and young professionals entering our field. It all starts with becoming a member of the Solid-State

Circuits Society where you can:

-Keep up with the latest trends and cutting-edge developments in our industry through our award-winning publications including “Solid-State Circuits Magazine” and “Journal of Solid State Circuits (JSSC)”.

-Access valuable career and educational tools - saving you both time and money with 24/7 access to our website and members-only professional development and educational material; Distinguished Lecturer Tours, Tutorials, and webinars by subject matter experts.

-Connect with your Peers - valuable networking opportunities through our world-class conferences, chapters, interactive educational offerings, and social media.

-Access exclusive SSCS Conference Digests for ISSCC, CICC, A-SSCC, ESSERC, and the Symposium on VLSI Technology and Circuits.

-Access publications - In addition to JSSC and the SSCS magazine, your SSCS membership gives you free access to IEEE Solid-State Circuits Letters, IEEE Sensors Magazine, IEEE Transactions on Circuits and Systems for Artificial Inelligence, and IEEE Transactions on AgriFood Electronics, plus discounted subscription rates to several other publications.

SSCS MEMBERSHIP SAVES EVEN MORE ON ISSCC REGISTRATION

This year, SSCS members will again receive an exclusive benefit of a $30 discount on the registration fee for ISSCC in addition to the IEEE discount. Also, the SSCS will again reward our members with a $10 Starbucks gift card when they attend the Conference as an SSCS member in good standing.

Join or renew your membership with IEEE’s Solid-State Circuits Society today at sscs.ieee.org - you will not want to miss out on the opportunities and benefits your membership will provide now and throughout your career.

ITEMS INCLUDED IN REGISTRATION

Technical Sessions & more: In person registration includes admission to all technical and evening sessions starting Sunday evening and continuing throughout Monday, Tuesday and Wednesday. Access to author interviews, social hours, to the Student Research Preview, to the Demo Sessions, to the open Women in Circuits Programs and to the Exhibition are also included. ISSCC does not offer partial conference registrations.

Technical Book Display: Several technical publishers will have collections of professional books and textbooks for sale during the Conference. The Book Display will be open on Monday from 3:00 pm to 8:00 pm; on Tuesday from 9:30 am to 1:30 pm; and on Tuesday from 3:00 pm to 8:00 pm.

Exhibition: For the third year, ISSCC is planning to organize an Exhibition open to Companies and non-academic Research Institutions. The main aim of the Exhibition is to showcase the participating Corporations/Institutions, their products and their applications. The Exhibition will be open on Monday from 3:00 pm to 8:00 pm; on Tuesday from 9:30 am to 1:30 pm; and on Tuesday from 3:00 pm to 8:00 pm.

Demonstration Sessions: Hardware demonstrations will support selected papers on Monday and Tuesday evenings.

Author Interviews: Author Interviews will be held Monday, Tuesday and Wednesday evenings. Authors from each day's papers will be available to discuss their work.

Monday and Tuesday Social Hours: Refreshments will be available starting at 5:30 pm.

University Events: Several universities are planning social events during the Conference. Check the University Events display at the conference for the list of universities, locations and times of these events.

Publications: All ISSCC registrants will be able to access online the Digital Digest and the registrations of the Technical Presentations Besides, Conference registration includes:

-Papers Visuals: The visuals from all papers presented will be available by download.

-Demonstration Session Guidebook: A descriptive guide to the Demonstration Session will be available by download.

-Note: Instructions will be provided for access to all downloads. Downloads will be available both during the Conference and for a limited time afterwards.

OPTIONAL EVENTS

Educational Events: Many educational events are available at ISSCC for an additional fee. There are ten 90-minute Tutorials and two all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. The Forums and Short Course include breakfast pastries and coffee, lunch and break refreshments. The Tutorials include break refreshments. See the schedule for details of the topics and times.

OPTIONAL PUBLICATIONS

ISSCC 2026 Publications: The following ISSCC 2026 digital publications can be purchased in advance or on site:

2026 ISSCC Download USB: All of the downloads included in conference registration, (regular papers and presentations) **(mailed in March)**

2026 Tutorials USB: All of the 90 minute Tutorials **(mailed in June).**

2026 Short Course USB: (mailed in June).
The Short Course and Tutorial USBs contain audio and written English transcripts synchronized with the presentation visuals. In addition, the USBs contain a pdf file of the presentations and pdf files of key reference material.

Earlier ISSCC Publications: Selected publications from earlier conferences can be purchased. There are several ways to purchase this material:

-Items listed on the registration website can be purchased with registration and picked up at the conference.

-Visit the ISSCC Publications Desk. This desk is located in the registration area and has the same hours as conference registration. With payment by cash, check or credit card, you can purchase materials at this desk. See the posted list at the Conference for titles and prices.

-Visit the ISSCC website at www.isscc.org and click on the link "SHOP/Shop ISSCC/Shop Now" where you can order online or download an order form to mail, email or fax. For a small shipping fee, this material will be sent to you immediately and you will not have to wait until you attend the Conference to get it.

HOW TO MAKE HOTEL RESERVATIONS

Online: ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott Marquis online. Go to the conference website and click on the Hotel Reservation link. ***Conference room rates are $291 for a single/double*** *(per night plus tax),* ***Student Room Rate is $222 for a single/double*** *(per night plus tax)***.** In addition, ISSCC attendees who are Bonvoy Members booked in the ISSCC group receive **in-room Internet access. Non-members of Bonvoy may sign up at check in, there is no charge for participation.**

All online reservations require the use of a credit card. Online reservations are confirmed immediately. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC. **Telephone:** Call 877- 622-3056 (US) or 415-896-1600 and ask for "Reservations." When making your reservation, identify the group as ISSCC 2025 to get the group rate.

Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than 5 pm Pacific Time January 26th, 2026 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. **Once this limit is reached or after January 26th, the group rates may no longer be available and reservations will be filled at the best available rate.** Changes: Before the hotel deadline, your reservation can be changed by calling the telephone numbers above. After the hotel deadline, call the Marriott Marquis at 415-896-1600 (ask for "Reservations"). Have your hotel confirmation number ready.

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IEEE is committed to the principle that all persons shall have equal access to programs, facilities, services, and employment without regard to personal characteristics not related to ability, performance, or qualifications as determined by IEEE policy and/or applicable laws.

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REFERENCE INFORMATION

Conference Website:	www.isscc.org
ISSCC Email:	ISSCC@ieee.org
Registration questions:	ISSCCinfo@yesevents.com
Hotel Information:	San Francisco Marriott Marquis Phone: 415-896-1600 780 Mission Street San Francisco, CA 94103
Press Information:	Laura C. Fujino Phone: 416-418-3034 University of Toronto Email: lcfujino@aol.com
Registration:	YesEvents Phone: 800-937-8728 Email: issccinfo@yesevents.com

Hotel Transportation

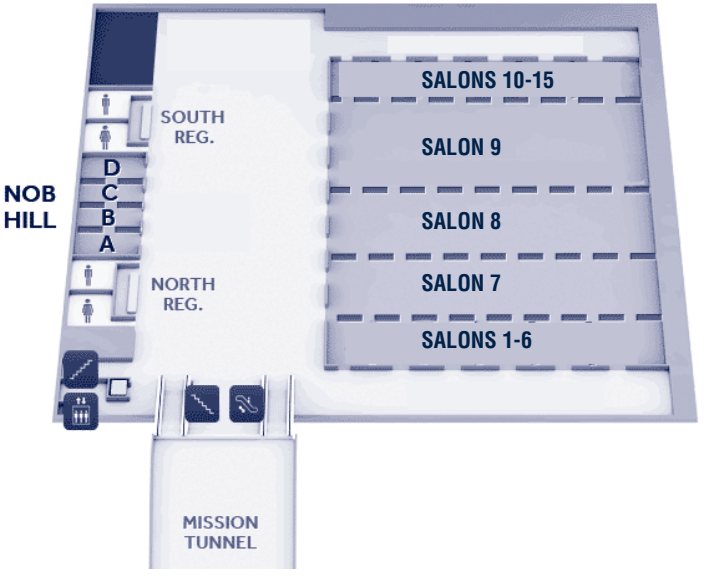
Visit the ISSCC website "Registration/Transportation from Airport" page for helpful travel information and links.
You can get a map and driving directions from the hotel website at:
www.marriott.com/hotels/travel/sfodt-san-francisco-marriott-marquis/

Next ISSCC Dates and Location:
ISSCC 2027 will be held on February 14-18, 2027
at the San Francisco Marriott Marquis Hotel.

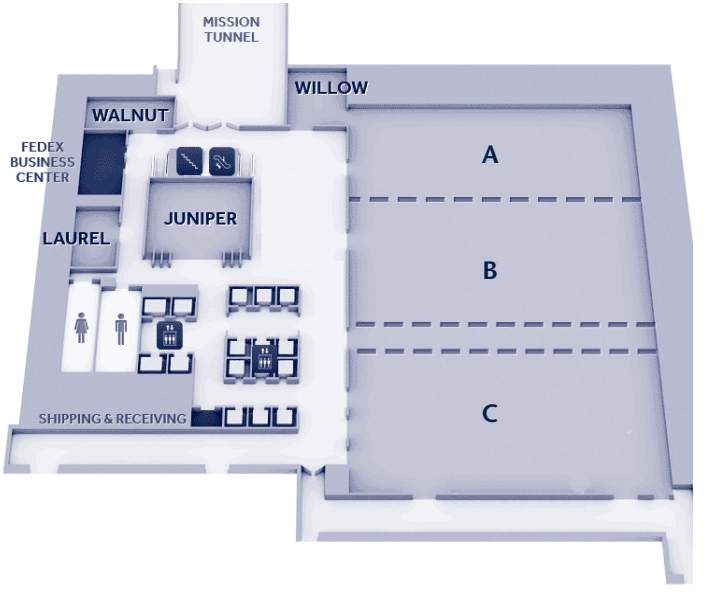
Subcommittee Chairs

Analog:	Viola Schaffer
Data Converters:	Jan Westra
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Digital Circuits:	Huichu Liu
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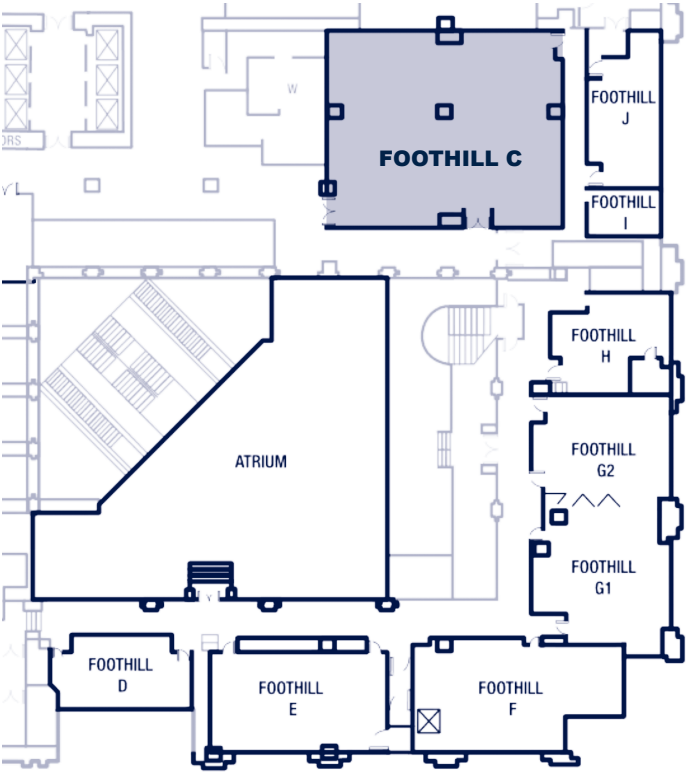
Lower B2 Level
Yerba Buena Ballroom



B2 Level
Golden Gate Hall



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